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28 December 2006

SEMICONDUCTOR DEVICES,  
HIGH RELIABILITY, SPACE USE,  
GENERAL SPECIFICATION FOR

JAXA  
JAPAN AEROSPACE EXPLORATION AGENCY

This specification was originally written and established in the Japanese language. This specification has been translated into English for international users. Note that this document is a working document for international users and is not subject to configuration control by JAXA. Any discrepancies found in this document should be verified against the latest Japanese document before any significant decisions are made.

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– i –
Revision Record			
Rev.	Date	Revised Contents	
NC	31 Mar. 03	Original	
A	31 Mar. 04	Revised with reorganization from NASDA to JAXA. - Renumbered the specification no. from “NASDA-QTS-2030” to “JAXA-QTS-2030”. - Reflected change of organization name to the text.	
B	28 Dec. 06	Change with revision to JAXA-QTS-2000C. - Paragraph 1.4: Changed “NASDA*****” to “JAXA*****” in part number definition. Corrected clerical errors and matched terminology in the text. - Changed the part number descriptions from “NASDA” to “JAXA” in entire text. - Paragraph 2.2: Reflected number change of JAXA Parts Application Handbook from “NASDA-HDBK-4” to ”JERG-0-035”.	

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– ii –
<b>Contents</b>			
1. GENERAL .....		1	
1.1 Scope .....		1	
1.2 Terms and Definitions .....		1	
1.3 Classification .....		1	
1.4 Part Number .....		1	
1.4.1 Radiation Hardness.....		1	
1.4.2 Constituent.....		2	
1.4.3 Identification Number .....		2	
1.4.4 Suffix Letter .....		2	
2. APPLICABLE DOCUMENTS .....		2	
2.1 Applicable Documents.....		2	
2.2 Reference Documents.....		2	
2.3 Order of Precedence .....		3	
2.4 Detail Specification .....		3	
2.4.1 Detail Specification Number .....		3	
2.4.2 Revision Letter of Detail Specification.....		3	
2.4.3 Independency of Detail Specification .....		3	
2.4.4 Format of Detail Specification .....		3	
3. REQUIREMENTS.....		3	
3.1 Certification .....		3	
3.1.1 Qualification Coverage.....		3	
3.1.2 Initial Qualification .....		4	
3.1.3 Retention of Qualification .....		4	
3.1.4 Effective Period of Certification .....		4	
3.1.5 Change of Qualification Coverage .....		4	
3.2 Quality Assurance Program .....		4	
3.2.1 Establishment of a Quality Assurance Program.....		4	
3.2.2 TRB Formation.....		4	
3.3 Design and Construction .....		5	
3.3.1 Operating Temperature.....		5	
3.3.2 Metallization .....		5	
3.3.3 Glassivation.....		6	
3.3.4 Thickness of Die.....		6	
3.3.5 Die Mounting and Plating .....		6	
3.3.6 Internal Lead Wire and Bonding Method.....		6	
3.3.7 Package .....		7	
3.3.8 Screw Threads .....		8	
3.4 Marking.....		9	
3.4.1 Marking Items.....		9	
3.4.2 Marking Location and Layout .....		10	
3.4.3 Marking Option.....		10	
4. QUALITY ASSURANCE PROVISIONS .....		10	
4.1 General Requirements .....		10	
4.2 Incoming Material Control .....		10	

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– iii –
4.2.1	Receiving Inspection .....	10	
4.2.2	Records of Incoming Material Control .....	11	
4.3	Manufacturing Process Control .....	11	
4.3.1	Task Control of Manufacturing Process .....	11	
4.3.2	Rework Control .....	14	
4.3.3	Environmental Control .....	14	
4.3.4	Water Purity .....	14	
4.3.5	Production Records .....	14	
4.4	Classification of Inspections and Tests .....	15	
4.5	In-Process Inspection .....	15	
4.5.1	In-Process Inspection Records .....	15	
4.6	Qualification Test .....	15	
4.6.1	Evaluation Devices or Samples .....	16	
4.7	Screening .....	16	
4.8	Quality Conformance Inspection .....	16	
4.9	Long-Term Storage .....	16	
4.9.1	Disposition of Lots Stored for a Long Term at the Manufacturer's Site .....	16	
4.9.2	Storage by Purchasers .....	16	
4.10	Change of Tests and Inspections .....	16	
5.	PREPARATION FOR DELIVERY .....	16	
5.1	Packaging .....	17	
5.2	Marking on Package .....	17	
6.	NOTES .....	17	
6.1	Notes for Manufacturer .....	17	
6.1.1	Preparation and Registration of Application Data Sheet .....	17	
6.2	Notes for Acquisition Officers .....	17	
6.2.1	Items to be Specified for Procurement .....	17	
6.2.2	Review of Application Data Sheet .....	18	
6.3	Terms and Definitions .....	18	
Appendix A			
Inspection Procedure of Wafer Lot			
Appendix B			
Procedure for Screening			
Appendix C			
Procedures for Qualification Test and Quality Conformance Inspection			
Appendix D			
Procedures for Sampling Test and Inspection			
Appendix E			
Preparation of Design Documents			
Appendix F			
Preparation of Detail Specification			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 1 –
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**SEMICONDUCTOR DEVICES,  
HIGH RELIABILITY, SPACE USE,  
GENERAL SPECIFICATION FOR**

1. GENERAL

1.1 Scope

This specification establishes the general requirements and quality assurance provisions for space use high reliability semiconductor devices (hereinafter referred to as "semiconductor devices") used for electronic equipment installed on spacecrafts. This specification complies with JAXA-QTS-2000 (Common Parts/Materials, Space Use, General Specification for) which was recently established to transition to the qualified manufacturing line system and replaces the following specifications.

NASDA-QTS-19500A    Discrete Semiconductor Device, Reliability Assured,  
Space Development Use, General Specification for

1.2 Terms and Definitions

The definitions for terms used herein are as shown in JAXA-QTS-2000, paragraph 6.3 of this specification and each appendix.

1.3 Classification

Semiconductor devices covered by this specification shall be classified by materials, construction, characteristics, and applications and named according to provisions of JEITA ED-4001.

1.4 Part Number

The part number shall consist of JAXA, radiation hardness, constituent, identification number and suffix letters as follows:

(Example)

JAXA <sup>(1)</sup>	R	–	2SC	–	4307	–	A
	↓		↓		↓		↓
	Radiation hardness		Constituent		Identification number		Suffix letter
	(paragraph 1.4.1)		(paragraph 1.4.2)		(paragraph 1.4.3)		(paragraph 1.4.4)

Note: <sup>(1)</sup>"JAXA" indicates the part is for space use and may be abbreviated "J".

1.4.1 Radiation Hardness

The radiation hardness shall be identified by a single capital letter and indicates the radiation hardness assurance level.

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 2 –
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<u>Letter</u>	<u>Radiation hardness assurance level</u>
M	30 Gy (Si) {3x10 <sup>3</sup> rad (Si)}
D	100 Gy (Si) {1x10 <sup>4</sup> rad (Si)}
P	300 Gy (Si) {3x10 <sup>4</sup> rad (Si)}
R	1,000 Gy (Si) {1x10 <sup>5</sup> rad (Si)}
F	3,000 Gy (Si) {3x10 <sup>5</sup> rad (Si)}
H	10,000 Gy (Si) {1x10 <sup>6</sup> rad (Si)}

Note: Values in parentheses { } are for reference only.

1.4.2    Constituent

The constituent shall be the combination of a one-digit number and a single or double capital letter(s), and assigned according to the types, polarity or application of the semiconductor devices as specified in JEITA ED-4001.

1.4.3    Identification Number

The identification number shall be consecutive numbers starting from 11 and assigned for each registration as specified in JEITA ED-4001.

1.4.4    Suffix Letter

Part changes shall be identified by a capital letter starting from A. "R" shall be additionally used for reverse characteristics diodes or thyristors. The suffix letter shall be assigned as specified in JEITA ED-4001.

2.    APPLICABLE DOCUMENTS

2.1    Applicable Documents

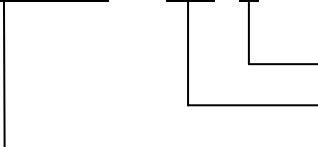
The documents listed below form a part of this specification to the extent specified herein. These documents are the latest issues available at the time of contract award or application. If it is necessary to designate an issue, the issue shall be specified in the detail specification.

a)	JAXA-QTS-2000	Common Parts/Materials, Space Use, General Specification for
b)	MIL-STD-750	Test Method Standard, Semiconductor Devices
c)	JIS B 0205	ISO General Purpose Metric Screw Threads Part1: Basic Profile to Part 4: Basic Dimensions
d)	JEITA ED-4001	Type Designation System for Discrete Semiconductor Devices
e)	ISO 14644-1:1999	Cleanrooms and Associated Controlled Environments --Part 1: Classification of Air Cleanliness
f)	ISO 14644-2:2000	Cleanrooms and Associated Controlled Environments -- Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1

2.2    Reference Documents

Following document is a reference document.

JERG-0-035	JAXA Parts Application Handbook
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JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 3 –
<p>2.3 Order of Precedence</p> <p>In the event of a conflict between the text of this specification and the applicable documents, the following order of precedence shall apply.</p> <ul style="list-style-type: none"> <li>a) Detail specification</li> <li>b) This specification</li> <li>c) JAXA-QTS-2000</li> <li>d) Applicable documents of this specification (paragraph 2.1, except for JAXA-QTS-2000)</li> </ul> <p>2.4 Detail Specification</p> <p>Detailed requirements for the type and performance of the semiconductor devices are specified in each detail specification.</p> <p>The detail specification shall be prepared and established by the manufacturer in accordance with Section A.4, Appendix A of JAXA-QTS-2000, and shall be registered with the Japan Aerospace Exploration Agency (hereinafter referred to as “JAXA”).</p> <p>2.4.1 Detail Specification Number</p> <p>The detail specification number shall be indicated in the following form in accordance with paragraph A.2.2.2, Appendix A of JAXA-QTS-2000.</p> <p>Example: <u>JAXA-QTS-2030</u> / <u>101</u> <u>A</u></p> <div style="margin-left: 200px;">  <div style="margin-left: 10px;"> <p>Revision letter</p> <p>Individual identification</p> <p>This specification number</p> </div> </div> <p>2.4.2 Revision Letter of Detail Specification</p> <p>A revision letter in the detail specification number shall be assigned in accordance with paragraph A.2.2.2.4, Appendix A of JAXA-QTS-2000.</p> <p>2.4.3 Independency of Detail Specification</p> <p>The detail specification shall be a stand-alone document with a unique number defined in accordance with paragraph 2.4.1.</p> <p>2.4.4 Format of Detail Specification</p> <p>The detail specification format shall be in accordance with Appendix F of this specification.</p> <p>3. REQUIREMENTS</p> <p>3.1 Certification</p> <p>3.1.1 Qualification Coverage</p> <p>Qualification shall be valid for semiconductor devices that are produced by the manufacturing line that conforms to design, construction, and materials specified in paragraph 3.3 and the quality assurance program. The qualification coverage shall be limited to the range of construction and designing limit values typified by evaluation</p>			



JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 4 –
<p>devices or samples which have passed the qualification test. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification.</p> <p>3.1.2 Initial Qualification</p> <p>To acquire certification of the semiconductor devices in compliance with this specification, a manufacturer shall establish a quality assurance program in accordance with paragraph 3.2.1, perform the qualification tests specified in paragraph 4.6, and acquire a certification status from JAXA as specified in paragraph 3.4.1 of JAXA-QTS-2000. The manufacturer shall be listed on the Qualified Manufacturers List of the Japan Aerospace Exploration Agency (JAXA QML).</p> <p>The manufacturer shall prepare design documents of the semiconductor devices to be qualified in accordance with Appendix E and submit them with Quality Assurance Program Plan at the time of application for qualification test.</p> <p>3.1.3 Retention of Qualification</p> <p>To continue supplying semiconductor devices in accordance with this specification, a manufacturer must apply for QML certification retention in accordance with paragraph 3.4.2.1 of JAXA-QTS-2000 commencing between 30 and 60 days prior to the expiration date of the certification period (paragraph 3.1.4).</p> <p>If products were not shipped during the effective period of certification and a quality conformance inspection was not conducted, the manufacturer may apply for retention of certification without conducting the quality conformance inspection.</p> <p>3.1.4 Effective Period of Certification</p> <p>The effective period of certification granted in compliance with this specification shall be three years.</p> <p>3.1.5 Change of Qualification Coverage</p> <p>To change the qualification coverage, the manufacturer shall perform procedures for re-qualification in accordance with paragraph 3.4.3 of JAXA-QTS-2000.</p> <p>3.2 Quality Assurance Program</p> <p>3.2.1 Establishment of a Quality Assurance Program</p> <p>To acquire certification in compliance with this specification, the manufacturer shall be responsible for establishing a quality assurance program that meets the requirements specified in paragraph 3.3.1 of JAXA-QTS-2000 and this specification. The manufacturer shall generate a Quality Assurance Program Plan in accordance with paragraph 3.3.2 of JAXA-QTS-2000 and provide the plan to JAXA for review in accordance with paragraph 3.3.6 of JAXA-QTS-2000.</p> <p>3.2.2 TRB Formation</p> <p>To acquire a certification status in compliance with this specification, the manufacturer shall form and operate the Technology Review Board (TRB) in accordance with paragraph 3.3.5 of JAXA-QTS-2000.</p>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 5 –
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3.3 Design and Construction

3.3.1 Operating Temperature

Unless otherwise specified in the detail specification, the minimum and maximum operating temperatures of the semiconductor devices shall be -55°C and +200°C, respectively.

3.3.2 Metallization

Unless otherwise specified in the detail specification, the metallization thickness shall be 0.80µm or more. The maximum allowable current densities shall not exceed the values specified below at any point of the metallized surface including the thinnest areas such as levels of the substrate.

Unit: A/cm<sup>2</sup>

Metallization material	Maximum allowable current density
Aluminum (99.99% pure or doped, without glassivation)	2x10 <sup>5</sup>
Aluminum (99.99% pure or doped, with glassivation)	5x10 <sup>5</sup>
Gold	6x10 <sup>5</sup>
All Others	2x10 <sup>5</sup> (Unless otherwise specified in the detail specification)

Maximum current densities shall be calculated using current and cross section areas which are determined as follows.

a)

The current shall be the maximum continuous current at the maximum load or equal to the simple time-averaged current obtained at the maximum rated frequency or duty cycle with the maximum load, whichever results in the greater current value. Currents shall be calculated on the assumption that currents flow uniformly through the conductor’s cross section driven by the maximum recommended operating voltage.

b)

The metallization thickness shall be the minimum allowed metallization thickness defined in the manufacturing specifications.

c)

The metallization width shall be an actual minimum design value (not mask widths) which is calculated in consideration of thinning and undercutting of the metal which is expected to occur during the etching process.

d)

Areas of barrier metals and nonconductive materials shall not be added to the cross section.

e)

To compensate for reduction of the cross section due to thinning, voids and scratches, the cross section shall be obtained from steps b) through d) and multiplied by 0.75.

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 6 –
<p>3.3.3      Glassivation</p> <p>Unless otherwise specified in the detail specification, silicon transistors shall be glassivated. The glassivation thickness shall be 0.40µm or more for SiO<sub>2</sub> and 0.20µm or more for Si<sub>3</sub>N<sub>4</sub>. The glassivation shall cover all conductor surfaces except for bonding pads.</p> <p>The spacing between all conductors that are not glassivated (e.g., spacing between bonding pads, bonding pads and scribed region) shall be 50µm or more.</p> <p>3.3.4      Thickness of Die</p> <p>Unless otherwise specified in the detail specification, thickness of dies shall be 150µm or more.</p> <p>3.3.5      Die Mounting and Plating</p> <p>Glass shall not be used for die mounting. When the bottom surface of the die is gold plated, the plating thickness shall be between 0.10µm and 1.00µm.</p> <p>3.3.6      Internal Lead Wire and Bonding Method</p> <p>a)    Internal lead wires</p> <p>Unless otherwise specified in the detail specification, the diameter of internal lead wires shall be 25µm as a minimum. For leads with a non-circular cross section, use a circular wire diameter which has the same cross section area. The material of the lead wires shall be the same metal used for the die metallization.</p> <p>b)    Bonding method</p> <p>All diodes, except the schottky barrier and point contact UHF diodes, shall be connected using metallurgical bonding (item v), paragraph 6.3).</p> <p>c)    Maximum allowable current</p> <p>Internal lead wires or other conductors which are in thermal contact with the die along their entire length shall be designed such that the maximum rated current (continuous current for DC, effective current for AC and peak current multiplied by <math>1/\sqrt{2}</math> for pulsed current) shall not exceed the maximum allowable current calculated by the following formula.</p> $I = \frac{1}{128} \times K \times d^{\frac{3}{2}}$ <p>Where:</p> <p>I = Maximum allowable current</p> <p>d = Wire/conductor diameter (When the cross section is not circular, the diameter of a circular wire or conductor of the same cross section area)</p> <p>K = A constant obtained from the length and composition of the wire or conductor as shown in Table 1.</p>			

**Table 1. Material and K Value**

Material	“K” value for bond-to-bond total conductor length	
	Length ≤ 1.0mm	Length > 1.0mm
Aluminum	22,000	15,200
Gold	30,000	20,500
Copper	30,000	20,500
Silver	15,000	10,500
Others	9,000	6,300

**3.3.7 Package****a) General**

The semiconductor device shall be hermetically sealed in a package made of glass, metal, ceramic or a combination of these materials.

No organic or polymer materials (e.g., lacquers, varnishes, coatings, adhesives, greases, etc.) or desiccants shall be used in the package.

**b) Package material**

External metal surfaces of the package shall be corrosion resistant. Nonmetallic materials of the package and coatings including markings shall be non-nutrient to fungus and shall not display blister, crack, outgas, softening, outflow or other defects under the specified test conditions.

**c) External lead material and finish****1) External lead material**

Unless otherwise specified in the detail specification, the external lead material composition shall meet one of the following material composition types.

**1.1) Type A**

Iron	53% nominal
Nickel	29±1%
Cobalt	17±1%
Manganese	0.65% max.
Carbon	0.06% max.
Silicon	0.20% max.
Aluminum	0.10% max.
Magnesium	0.10% max.
Zirconium	0.10% max.
Titanium	0.10% max.

(The summation of aluminum, magnesium, zirconium, and titanium contents shall not exceed 0.20%.)

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 8 –
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1.2) Type B

Nickel	40 to 43%
Manganese	0.80% max.
Silicon	0.30% max.
Carbon	0.10% max.
Chrome	0.25% max.
Cobalt	0.50% max.
Phosphorus	0.025% max.
Sulfur	0.025% max.
Aluminum	0.10% max.
Iron	Remainder

1.3) Type C

Nickel	41 to 43%
Manganese	0.75 to 1.25% max.
Silicon	0.30% max.
Carbon	0.10% max.
Sulfur	0.02% max.
Phosphorus	0.02% max.
Iron	Remainder

2) External lead finish

Unless otherwise specified in the detail specification, the external lead finish shall be one of the following options.

2.1) Solder dip

The solder dip shall be homogeneous with the minimum thickness at the major flats of 5.08µm solder (Sn60 to Sn63) over a primary finish in accordance with type 2.2) or 2.3) below, or nickel plating of a thickness between 2.54 and 7.62µm.

2.2) Acid tin plating

Acid tin plating thickness shall be between 2.54µm and 12.7µm. Nickel or copper under-plating (electroless or electrolysis) may be used. In this case, the under-plating shall be between 0.25µm and 7.62µm.

Remark: It is known that there are different tin platings with different compositions and reflectances. However, the acid tin plating specified herein shall be uniform and dense, and satisfy all the requirements specified herein.

2.3) Gold plating

The purity of gold shall be a minimum of 99.7% (i.e., a total of impurities and other metals shall not exceed 0.3%). The thickness of the plating shall be a minimum of 1.27µm. This finish requires electrolysis nickel or copper undercoating with a thickness between 1.27µm and 7.62µm.

3.3.8 Screw Threads

If screw threads are specified as one of the mechanical requirements, the screw threads shall meet standard screw threads specified in JIS B 0205-1 to JIS B 0205-4.

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 9 –
<p>3.4 Marking</p> <p>3.4.1 Marking Items</p> <p>Unless otherwise specified in the detail specification, the following marking items shall be placed on each product.</p> <ul style="list-style-type: none"> <li>a) Index and polarity (paragraph 3.4.1.1)</li> <li>b) Part number (paragraph 3.4.1.2)</li> <li>c) Inspection lot identification code (paragraph 3.4.1.3)</li> <li>d) Serial number (paragraph 3.4.1.4)</li> <li>e) Manufacturer's identification (paragraph 3.4.1.5)</li> </ul> <p>If there is insufficient surface area for the required markings, marking items may be omitted in the following order of priority.</p> <ul style="list-style-type: none"> <li>a) "JAXA" or "J" of part number</li> <li>b) "Constituent" of part number. Last capital letter must be marked.</li> <li>c) Serial number. In this case, attach a tag to the lead or body of the product.</li> </ul> <p>3.4.1.1 Index and Polarity Marking</p> <p>The index and polarity marking shall meet the following requirements. The manufacturer's identification shall not be used for this purpose. These items shall be visible from the top when the product is mounted in a normal manner.</p> <ul style="list-style-type: none"> <li>a) Index <ul style="list-style-type: none"> <li>The index indicates the start of lead numbers or mechanical orientation and shall be shown by a stamp, tab, notch or groove, among other means.</li> </ul> </li> <li>b) Polarity of diodes <ul style="list-style-type: none"> <li>The polarity of diodes shall be marked in one of the following ways. <ul style="list-style-type: none"> <li>1) A diode symbol or arrow pointing toward the cathode terminal in forward bias.</li> <li>2) A noticeable color band or a dot close to the cathode terminal in forward bias.</li> </ul> </li> </ul> </li> <li>c) Polarity of thyristor <ul style="list-style-type: none"> <li>A graphic symbol of the thyristor with an arrow indicating the direction of cathode terminal.</li> </ul> </li> </ul> <p>3.4.1.2 Part Number</p> <p>The part number shall be as specified in paragraph 1.4.</p> <p>3.4.1.3 Inspection Lot Identification Code</p> <p>An inspection lot identification code shall be assigned to each inspection lot (item p) of paragraph 4.3.1).</p> <p>3.4.1.4 Serial Number</p> <p>A serial number shall be assigned to each semiconductor device in the inspection lot prior to the radiographic inspection in the screening test (paragraph 4.7).</p> <p>3.4.1.5 Manufacturer's Identification</p> <p>The manufacturer's identification identifies the certified manufacturer. Manufacturer's name, abbreviated name, trademark or any combination of them shall be marked.</p>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 10 –
<p>3.4.2      Marking Location and Layout</p> <p>Unless otherwise specified in the detail specification, markings including the part number, inspection lot identification code, and serial number shall be placed on the surface which is visible when the product is mounted in a normal manner. The marking items may be placed in any layout as long as they function properly and do not interfere with any other markings.</p> <p>3.4.3      Marking Option</p> <p>The manufacturer shall complete marking on all products in the inspection lot by the end of the screening test or shall mark on only the samples used for Groups B, C, D and E tests of the qualification test or quality conformance inspection. When the manufacturer chooses the latter, the procedure shall be as follows.</p> <ul style="list-style-type: none"> <li>a)    Samples shall be marked prior to the Groups B, C, D, and E tests of the qualification test or quality conformance inspection.</li> <li>b)    Confirm that all markings meet all requirements upon completion of the test.</li> <li>c)    Mark on the products in the same inspection lot as samples and perform the external visual inspection as part of the screening test. The marking materials and processes shall be the same as those applied to the samples.</li> </ul> <p>4.      QUALITY ASSURANCE PROVISIONS</p> <p>4.1      General Requirements</p> <p>The manufacturer shall be responsible for implementing the quality assurance program specified in paragraph 3.2 of this specification and operating the TRB.</p> <p>4.2      Incoming Material Control</p> <p>Incoming materials shall be subjected to an appropriate receiving inspection and controlled to ensure that each material is traceable to the receiving inspection lot. The manufacturer shall establish and implement procedures to store and distribute incoming materials and to remove life limited materials.</p> <p>4.2.1      Receiving Inspection</p> <p>Receiving inspection for each incoming materials shall include at least the following items shown in Table 2.</p>			

**Table 2. Materials and Items for Receiving Inspection**

Material	Receiving inspection item
Substrates	Thickness, flatness, parallelism, dislocation density, plane direction, specific resistance, and visual inspection
Wire	Composition, uniformity, hardness, diameter, elongation, tensile strength, purity, and cleanliness
Packaging and lead materials	Dimensions, composition, strength, purity, and plating
Other metals	Composition and purity
Chemicals and gasses	Composition, purity, and grade
Masks	Configuration (width and length), pinholes (density, size, and distribution), scratches, and roughness of edges

#### 4.2.2 Records of Incoming Material Control

The records of incoming materials shall be classified into a) Incoming inspection records and b) storage, distribution and disposal records.

##### a) Incoming inspection records

- 1) Material name
- 2) Inspection items
- 3) Lot size
- 4) Lot identification code
- 5) Document number and established date of inspection instructions
- 6) Pass/fail of each lot and quantity of failed materials
- 7) Date of inspection and name or identification code of the inspector

##### b) Storage, distribution and disposal records

- 1) Material name
- 2) Storage conditions
- 3) Lot identification code
- 4) Storage date and quantity of storage materials
- 5) Distribution date, quantity, and lot identification code of finished/semi-finished products for which the material is used.
- 6) Disposal date

#### 4.3 Manufacturing Process Control

The manufacturer shall establish and maintain procedures, control parameters, and control methods of manufacturing processes.

##### 4.3.1 Task Control of Manufacturing Process

The manufacturer shall define and control each manufacturing process including at a minimum the items listed below. Rework shall be performed in accordance with paragraph 4.3.2. The manufacturer shall also establish and implement a storage method for finished or semi-finished products between processes. Following die



JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 12 –
<p>mounting process (item k)), the manufacturer shall perform additional sampling visual inspection in 100% visual inspection process.</p> <ul style="list-style-type: none"> <li>a) Wafer lot formation <ul style="list-style-type: none"> <li>1) Formation procedure for wafer lots</li> <li>2) Assignment method of wafer lot identification codes</li> </ul> </li> <li>b) Oxidation process <ul style="list-style-type: none"> <li>1) Oxide layer materials</li> <li>2) Forming method</li> <li>3) Control methods of oxide layer thickness, and pinhole/crack dimensions and density</li> <li>4) Furnace control method</li> </ul> </li> <li>c) Pattern formation process <ul style="list-style-type: none"> <li>1) Forming method</li> <li>2) Etching method</li> <li>3) Visual inspection method</li> </ul> </li> <li>d) Epitaxial growth process <ul style="list-style-type: none"> <li>1) Materials</li> <li>2) Forming method</li> <li>3) Pretreatment procedure of wafer</li> <li>4) Conditions</li> <li>5) Methods of inserting and extracting wafer</li> <li>6) Control methods of epitaxial layer thickness, sheet resistance and number of stacking faults</li> <li>7) Cleaning methods and frequency for susceptors and tubes</li> </ul> </li> <li>e) Junction formation process <ul style="list-style-type: none"> <li>1) Dope source</li> <li>2) Forming method</li> <li>3) Control method of diffusion depth</li> </ul> </li> <li>f) Metallization formation process <ul style="list-style-type: none"> <li>1) Metallization materials</li> <li>2) Forming method</li> <li>3) Forming conditions</li> <li>4) Sinter conditions</li> <li>5) Inspection method specified in Appendix A</li> <li>6) Cleaning method and frequency for chamber</li> </ul> </li> <li>g) Glassivation formation process <ul style="list-style-type: none"> <li>1) Forming material</li> <li>2) Forming method</li> <li>3) Conditions</li> <li>4) Control method of dope concentration</li> <li>5) Inspection method specified in Appendix A</li> </ul> </li> <li>h) Back surface polishing process <ul style="list-style-type: none"> <li>1) Materials</li> <li>2) Polishing methods</li> <li>3) Polishing conditions</li> <li>4) Protection method of front surface</li> <li>5) Removing and cleaning method of protective coating</li> </ul> </li> </ul>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 13 –
<div data-bbox="309 230 1455 2051"> <ul style="list-style-type: none"> <li>6) Control method of parallelism</li> <li>7) Inspection method specified in Appendix A</li> <li>i) Scribing and dicing process               <ul style="list-style-type: none"> <li>1) Scribing method</li> <li>2) Dicing method</li> <li>3) Method of 100% visual inspection: The criteria of 100% visual inspection shall be as specified in the test methods 2069, 2070, 2072 and 2073 of MIL-STD-750.</li> </ul> </li> <li>j) Formation of production lots               <ul style="list-style-type: none"> <li>1) Formation method of production lots<sup>(1)</sup></li> <li>2) Assignment method of production lot identification code</li> </ul> <p>Note: <sup>(1)</sup> It is desirable that the production lot is prepared such that inspection sublots can be easily organized (item o) of paragraph 4.3.1).</p> </li> <li>k) Die mounting process               <ul style="list-style-type: none"> <li>1) Materials of mounting and mounting area of package</li> <li>2) Mounting structure</li> <li>3) Conditions</li> <li>4) Method of 100% visual inspection: The criteria of 100% visual inspection shall be as specified in test methods 2069, 2070, 2072 and 2073 of MIL-STD-750.</li> <li>5) Control method of adhesive strength</li> </ul> </li> <li>l) Interconnect bonding process               <ul style="list-style-type: none"> <li>1) Materials</li> <li>2) Lead type</li> <li>3) Bonding method</li> <li>4) Bonding conditions</li> <li>5) Method of 100% visual inspection: The criteria of 100% visual inspection shall be as specified in test methods 2069, 2070, 2072 and 2073 of MIL-STD-750. This inspection may be included in item m) below.</li> <li>6) Control method of bond strength</li> </ul> </li> <li>m) Pre-cap visual inspection process The procedure and criteria of the visual inspection shall be as specified in test methods 2069, 2070, 2072 and 2073 of MIL-STD-750.</li> <li>n) Sealing process               <ul style="list-style-type: none"> <li>1) Package and sealing materials</li> <li>2) Sealing method</li> <li>3) Pre-sealing stabilization bake</li> <li>4) Sealing conditions</li> </ul> </li> <li>o) Formation of inspection sublots               <ul style="list-style-type: none"> <li>1) Formation method of inspection sublots<sup>(1)</sup></li> <li>2) Assignment method of inspection subplot identification code</li> </ul> <p>Note: <sup>(1)</sup> Inspection sublots shall meet the following requirements.</p> <ul style="list-style-type: none"> <li>i) An inspection subplot shall consist of semiconductor devices with identical die design, package type and lead finish.</li> </ul> </li> </ul> </div>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 14 –
<div data-bbox="453 230 1426 663"> <ul style="list-style-type: none"> <li>ii) An inspection subplot shall be manufactured using dies from a single wafer lot.</li> <li>iii) Semiconductor chips shall be made on a die produced from a single wafer lot.</li> <li>iv) Each assembly process shall be completed using the same machines during a single shift. The die mounting and lead bonding shall be performed during 2 and 4 shifts, respectively.</li> <li>v) All assembly operations from die mounting through package sealing shall be completed within the same 6-week period.</li> <li>vi) Each inspection lot shall consist of 1,000 semiconductor devices maximum.</li> </ul> </div> <div data-bbox="309 669 734 703"> <p>p) Formation of inspection lots</p> </div> <div data-bbox="368 705 1152 784"> <ul style="list-style-type: none"> <li>1) Formation method of inspection lots<sup>(1)</sup></li> <li>2) Assignment method of inspection lot identification code</li> </ul> </div> <div data-bbox="368 792 1174 831"> <p>Note: <sup>(1)</sup> Inspection lots shall meet the following requirements.</p> </div> <div data-bbox="453 842 1420 1039"> <ul style="list-style-type: none"> <li>i) An inspection lot shall consist of semiconductor devices with identical die design, package type and lead finish.</li> <li>ii) An inspection lot shall consist of five sublots as a maximum.</li> <li>iii) All assembly operations from die mounting through package sealing shall be completed within the same 8-week period.</li> </ul> </div> <div data-bbox="186 1075 515 1108"> <p>4.3.2 Rework Control</p> </div> <div data-bbox="306 1122 1455 1357"> <p>Rework shall be documented in work records for the production process in accordance with paragraph 4.3.5. Reworked products shall be clearly distinguished from other products. Reworks on the metallization, oxidizing, glassivation, and all assembly processes prior to sealing processes shall not be performed. Once sealed, rework shall be limited to re-cleaning, correction of defective marking, and lead straightening (e.g., reshaping of lead tips which does not affect hermeticity of the product).</p> </div> <div data-bbox="186 1393 604 1426"> <p>4.3.3 Environmental Control</p> </div> <div data-bbox="306 1442 1455 1594"> <p>Temperature, relative humidity, and air cleanliness shall be controlled for manufacturing processes such as wafer manufacturing and assembly operations which are significantly affected by the environment. The air cleanliness shall be measured in accordance with ISO 14644-1 and 14644-2.</p> </div> <div data-bbox="186 1630 477 1666"> <p>4.3.4 Water Purity</p> </div> <div data-bbox="306 1680 1450 1796"> <p>The purity of water shall be controlled with respect to the minimum specific resistivity, maximum total solids, maximum organic impurity, maximum bacteria concentration and maximum chlorine contents at room temperature.</p> </div> <div data-bbox="186 1830 572 1865"> <p>4.3.5 Production Records</p> </div> <div data-bbox="306 1879 1450 2033"> <p>Production records shall be categorized as either a) work records for the production process or b) control records such as for environmental conditions. Production records shall be managed in accordance with the quality assurance program specified in paragraph 3.2.1 and include at least the following items.</p> </div>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 15 –
<div data-bbox="309 230 1452 703"> <ul style="list-style-type: none"> <li>a) Work records for the production process               <ul style="list-style-type: none"> <li>1) Name of work</li> <li>2) Lot identification code of materials and products (including semi-finished products)</li> <li>3) Document number and established date of work instructions</li> <li>4) Quantity of incoming and outgoing products (including semi-finished products) for each work and their disposition</li> <li>5) Date of work and name or identification code of operator</li> <li>6) Identification of equipment used</li> </ul> </li> <li>b) Control records such as for environmental conditions               <ul style="list-style-type: none"> <li>1) Document number and established date of control instruction</li> <li>2) Date of measurement and name or identification code of operator</li> </ul> </li> </ul> </div> <div data-bbox="188 741 783 775"> <p>4.4 Classification of Inspections and Tests</p> </div> <div data-bbox="279 788 1415 862"> <p>Inspections and tests shall include screening in addition to three categories specified in paragraph 4.3 of JAXA-QTS-2000.</p> </div> <div data-bbox="279 869 751 1021"> <ul style="list-style-type: none"> <li>a) In-process inspection</li> <li>b) Qualification test</li> <li>c) Screening test</li> <li>d) Quality conformance inspection</li> </ul> </div> <div data-bbox="188 1059 564 1093"> <p>4.5 In-Process Inspection</p> </div> <div data-bbox="279 1106 1457 1379"> <p>The manufacturers shall perform the in-process inspections during the manufacturing process to detect any failure which could seriously affect the reliability and quality of the products, assure the workmanship, and characterize properties which cannot be measured from the finished products. The manufacturer shall perform wafer lot inspection specified in Appendix A and other in-process inspections such as those listed below. The manufacturing flow chart in the Quality Assurance Program Plan shall define the inspection process.</p> </div> <div data-bbox="279 1386 1110 1621"> <ul style="list-style-type: none"> <li>a) Internal visual inspection of semi-finished products (non-destructive, 100% or sampled inspection)</li> <li>b) Physical and chemical inspection of semi-finished products (destructive or non-destructive, sampled inspection)</li> <li>c) Characterization of semi-finished products (non-destructive, 100% or sampled inspection)</li> </ul> </div> <div data-bbox="188 1659 713 1693"> <p>4.5.1 In-Process Inspection Records</p> </div> <div data-bbox="309 1706 1404 1780"> <p>The manufacturer shall control in-process inspection records in accordance with the quality assurance program specified in paragraph 3.2.1.</p> </div> <div data-bbox="188 1818 510 1852"> <p>4.6 Qualification Test</p> </div> <div data-bbox="279 1865 1457 1980"> <p>The qualification test shall be performed on inspection lots which have passed screening test in accordance with Appendix C using the evaluation devices or samples produced using the same design, construction, materials and manufacturing line as those to be qualified.</p> </div>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 16 –
<p>4.6.1 Evaluation Devices or Samples</p> <p>Evaluation devices or samples shall be produced using the manufacturing line that satisfies designs, constructions and materials requirements defined in the Quality Assurance Program Plan and shall have the ability of proving that the manufacturing line to be certified has an adequate capability with respect to the structure and design limits of the products.</p> <p>4.7 Screening</p> <p>To supply semiconductor devices in compliance with this specification, screening shall be conducted in accordance with Appendix B. Prior to screening, production lots (item j) of paragraph 4.3.1) shall be re-grouped into inspection lots (item o) of paragraph 4.3.1). Screenings may be performed anytime after the final sealing process has been completed. In addition, each product shall be marked with a unique serial number within the inspection lot prior to the radiograph inspection to provide traceability between each measurement and individual product.</p> <p>4.8 Quality Conformance Inspection</p> <p>The quality conformance inspection is defined as a lot assurance inspection for delivery. It shall be performed in accordance with Appendix C for inspection lots which passed the screening test. Only those semiconductor devices that passed the quality conformance inspection are considered in compliance with this specification and allowed to be delivered. Products selected as samples shall be handled as specified in paragraph C.3.5, Appendix C.</p> <p>4.9 Long-Term Storage</p> <p>4.9.1 Disposition of Lots Stored for a Long Term at the Manufacturer's Site</p> <p>When products have been stored at the manufacturer's site for 24 months or longer after the quality conformance inspection, the manufacturer shall repeat the Group A quality conformance inspection and the 100% visual inspection prior to delivery. Only the products that have passed such tests can be shipped as products. If products fail in any subgroup inspection, 100% inspection shall be performed for items in that subgroup. Only the semiconductor devices that have passed the inspection can be shipped as products. Failed products shall be removed and shall not be delivered. The date of re-inspection shall be marked on the package or storage box.</p> <p>4.9.2 Storage by Purchasers</p> <p>The conditions and period of storage by purchasers shall be specified in the detail specification, if necessary.</p> <p>4.10 Change of Tests and Inspections</p> <p>Any change in the in-process inspection, screening test or quality conformance inspection specified in this specification shall be made in accordance with paragraphs 4.4 and 6.1 of JAXA-QTS-2000.</p> <p>5. PREPARATION FOR DELIVERY</p> <p>Preparation for delivery shall be as follows and as specified in Section 5 of JAXA-QTS-2000.</p>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 17 –
<p>5.1 Packaging</p> <p>Prior to delivery, the products shall be packaged individually. The package shall hold the products securely and prevent direct impact on the products. The package shall protect the products from moisture and be free from any sharp edge or burr on the external surfaces. It is desirable that the package allows visual inspection. The packaging material shall not break, peel off, crumble, loosen, accumulate static electricity, or corrode. Tape or adhesives shall not be used to secure the products. Special care shall be given to the products which require protection against electrostatic discharge. Individual shipping packages shall be kept in a shipping container to protect the products from possible damage during shipment.</p> <p>5.2 Marking on Package</p> <p>Each shipping package shall have the markings as specified in items b) through e) of paragraph 3.4.1. However, when the markings on the products are clearly visible in a packaged configuration, those markings on the package may be omitted. For packages with anti-electrostatic measures, a marking item “ESD sensitive” shall be added. All markings shall be waterproof. When individual packages are kept in a shipping container, marking items on the individual packages shall be duplicated on the container except for marking item d). Quantity, contract (order) number, applicable specification number, date of packaging and inspection result shall be added as the marking items.</p> <p>6. NOTES</p> <p>6.1 Notes for Manufacturer</p> <p>6.1.1 Preparation and Registration of Application Data Sheet</p> <p>The manufacturer shall prepare the application data sheet in accordance with Appendix G of JAXA-QTS-2000 and register it with JAXA.</p> <p>6.2 Notes for Acquisition Officers</p> <p>6.2.1 Items to be Specified for Procurement</p> <p>To purchase semiconductor devices manufactured in compliance with this specification, the purchaser shall provide the following information.</p> <ul style="list-style-type: none"> <li>a) Part number</li> <li>b) This specification number</li> <li>c) Detail specification number</li> <li>d) Indication of test data or source inspection results to be submitted for delivery</li> <li>e) Others</li> </ul> <p>Requirements other than those defined in this specification may be specified for special applications as item e). However, if the requirements conflict with the existing requirements in this specification, the purchaser shall not request the manufacturer to indicate that the semiconductor devices complies with this specification.</p>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 18 –
<p>6.2.2    Review of Application Data Sheet</p> <p>The application data sheet details additional product information necessary for parts selection and designing that is not contained in the detail specification such as the qualification test data. The acquisition officers are requested to carefully review the Application Data Sheet prior to acquisition.</p> <p>6.3    Terms and Definitions</p> <p>a)    Absolute maximum rating</p> <p>The values specified as "ratings", "maximum ratings", or "absolute maximum ratings" are based on the "absolute system." Unless a specific test method is required, the values shall not be exceeded under any operating or test conditions. Unless otherwise specified, the voltage, current and power ratings are determined based on continuous DC power conditions with unconstrained thermal radiation at an ambient temperature of +25°C. For pulsed or similar operating conditions, the current, voltage, and power loss ratings are functions of time and duty cycle.</p> <p>b)    Breakdown voltage</p> <p>The breakdown voltage is the maximum instantaneous voltage, including repetitive and non-repetitive transients, which can be applied across a junction in the reverse direction without limiting the current by an external means (circuit). Breakdown voltage is also an instantaneous voltage which occurs during a transition from a small-signal high impedance region to a small-signal low impedance region.</p> <p>c)    Constant current source</p> <p>A constant current source is a current source that does not cause any measurement changes greater than the required measurement precisions when the generator impedance is halved.</p> <p>d)    Constant voltage source</p> <p>A constant voltage source is a voltage source that does not cause any measurement changes greater than the required measurement precisions when the generator impedance is doubled.</p> <p>e)    Noise figure</p> <p>The noise figure of a given frequency is a ratio of the total noise power per unit bandwidth (determined by the output frequency) at the output to the noise power of the frequency at the input.</p> <p>The noise temperature at the input is 293°K at all frequencies.</p> <p>f)    Open circuit</p> <p>An open circuit is a circuit that does not cause any measurement changes greater than the required measurement precisions when the terminating impedance is halved.</p> <p>g)    Pulse</p> <p>A pulse is a flow of electrical energy of short duration. Figure 1 shows an illustrative explanation of the characteristics defined in items h) through m).</p>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 19 –
<div data-bbox="199 280 1460 918"> <p> <math>t_r</math> = Pulse rise time  <math>t_d</math> = Pulse delay time  <math>t_p</math> = Pulse time  <math>t_s</math> = Pulse storage time  <math>t_f</math> = Pulse fall time  <math>t_w</math> = Pulse average time  <math>l</math> = Pulse amplitude </p> <p>Notes:  1: Subscript 1 denotes input.  2: Subscript 2 denotes output. </p> </div>			
<b>Figure 1. Pulse Measurements</b>			
<p>h) Pulse average time The average pulse time is the time from a point where the amplitude of the pulse has risen to 50% of the maximum amplitude to a point where the amplitude of the pulse has fallen to 50% of the maximum amplitude.</p> <p>i) Pulse delay time The delay time is the time from a point where the amplitude of the input pulse has risen to 10% of its maximum amplitude to a point where the amplitude of the output pulse has risen to 10% of its maximum amplitude.</p> <p>j) Pulse fall time The fall time is the time that the pulse amplitude takes to decrease from 90% to 10% of the maximum amplitude.</p> <p>k) Pulse rise time The rise time is the time that the pulse amplitude takes to increase from 10% to 90% of the maximum amplitude.</p> <p>l) Pulse storage time The storage time is a time from a point where the amplitude of the input pulse has decreased to 90% of its maximum amplitude to a point where the amplitude of the output pulse has decreased to 90% of its maximum amplitude.</p> <p>m) Pulse time The pulse time is the time between 90% of amplitude on the leading edge and 90% of amplitude of the trailing edge.</p> <p>n) Short circuit A short circuit is a circuit that does not cause any measurement changes greater than the required measurement precisions when the terminating impedance is doubled.</p>			



JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 20 –
<p>o) Small signal A small signal is a signal that does not cause any measurement changes greater than the required measurement precisions when the signal amplitude is doubled.</p> <p>p) Ambient temperature Ambient temperature is the air temperature measured under a semiconductor device in an environment of sufficiently uniform temperature, cooled only by natural air convection and not practically affected by reflection or radiation.</p> <p>q) Case temperature Case temperature is the temperature measured at a specified point on the case of a product.</p> <p>r) Storage temperature Storage temperature is the temperature at which the semiconductor devices can be stored without any applied power.</p> <p>s) Thermal equilibrium Thermal equilibrium is a state that does not cause any measurement changes greater than the required measurement precisions when the test duration is doubled.</p> <p>t) Thermal resistance Thermal resistance is a temperature rise per unit power consumption at the junction with respect to an external temperature reference in thermal equilibrium.</p> <p>u) Package type A package type is characterized by the case outline, configuration, materials (including bonding wire, ribbon and die attach), piece parts (excluding preforms which differ only in size) and assembly processes.</p> <p>v) Metallurgical bond Metallurgical bond is a bond of constituent materials (metals or semiconductors) achieved by solidification of the constituent materials after re-growth and re-crystallization of the materials under a temperature and pressure where eutectic melt, normal melt, or solid diffusion of the materials occurs.</p> <p>w) Production lot A production lot is a group of semiconductor devices manufactured (or in the middle of the manufacturing process) on the same production line using the same manufacturing technology, materials, controls and design.</p> <p>x) Inspection lot An inspection lot is a group of semiconductor devices with the same die design, package type and lead finish. Inspection lots are usually divided into inspection sublots.</p> <p>y) Inspection subplot An inspection subplot is a group of products with the same die design, package type, and lead finish. Inspection sublots are processed together at all production processes.</p> <p>z) Final seal The final seal is a manufacturing process, after which access to internal elements of the product is not possible unless it is disassembled.</p>			

JAXA-QTS-2030B 28 December 2006	J A X A Parts Specification	Page	– 21 –
<p data-bbox="279 232 486 264">aa) Delta limits</p> <p data-bbox="339 273 1433 344">A delta limit is the maximum allowable deviation of a parameter from an acceptance criteria of a given test.</p> <p data-bbox="339 360 1420 472">Remark: Delta limit given as a percentage value means that the deviation of the parameter is calculated as a percentage of the post test measurement to the pre test measurement.</p> <p data-bbox="279 481 462 512">ab) Wafer lot</p> <p data-bbox="339 521 1185 553">A wafer lot is a group of wafers formed together at each process.</p> <p data-bbox="279 562 798 593">ac) Percent Defective Allowable (PDA)</p> <p data-bbox="339 602 775 633">The PDA is allowable failure rate.</p> <p data-bbox="279 642 478 674">ad) Inspection</p> <p data-bbox="339 683 1428 754">The inspection is a process to judge acceptance in a simple manner by comparison to specifications or limit samples.</p> <p data-bbox="279 763 395 795">ae) Test</p> <p data-bbox="339 804 1433 916">A test is a process to obtain measurement data, judge acceptance, and evaluate workmanship of the product totally based on large or small, distribution, deviation of obtained data, and series of test data.</p>			