ECSS-Q-70-38A
26 October 2007

Space product assurance

High-reliability soldering for surface-mount and mixed technology

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

Published by: ESA Requirements and Standards Division
ESTEC, P.O. Box 299,
2200 AG Noordwijk,
The Netherlands

ISSN: 1028-396X

Price: € 30

Printed in: The Netherlands

Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards.

Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

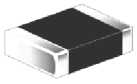
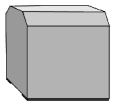
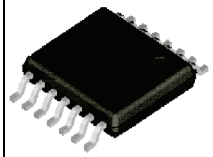
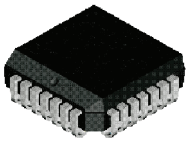
The formulation of this Standard takes into account the existing ISO 9000 family of documents.

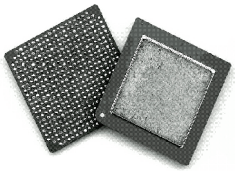
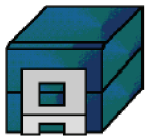
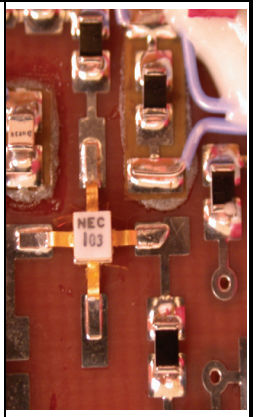
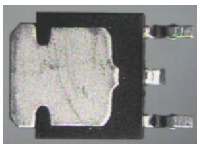
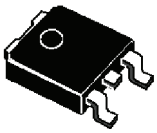
This Standard has been prepared by the ECSS-Q-70-38 Working Group, reviewed by the former ECSS Product Assurance Panel and the ECSS Executive Secretriat and approved by the ECSS Technical Authority.

(This page is intentionally left blank)

Introduction

This Standard prescribes requirements for electrical connections of leadless and leaded surface mounted devices (SMD) on spacecraft and associated equipment, utilising a range of substrate assemblies and employing solder as the interconnection media. The principal types of SMDs can be gathered in the following families:

Rectangular and square end-capped or end-metallized device with rectangular body e.g. end capped chip resistors and end capped chip capacitors.	
Bottom terminated chip device This type of device has metallised terminations on the bottom side only.	
Cylindrical or square end-capped devices with cylindrical body e.g. MELF.	
Castellated chip carrier device The main component of this type is leadless ceramic chip carrier (LCCC).	
Device with round, flattened, ribbon "L" and gull-wing leads e.g. small-outline transistor (SOT), small-outline package (SO), flat pack and quad flat pack (QFP). This family also comprises devices for through-hole mounting that have been reconfigured to surface mounting.	
"J" leaded device e.g. ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC).	

Area array devices These devices are leadless (no leads). The interconnections between solder pads on the devices and solder pads on the PCB consist entirely of solder. The devices have either solder balls (Ball Grid Array – BGA) or solder columns (Column Grid Array – CGA) applied to the solder pads on the devices prior to mounting on a PCB (normally done by the device manufacturer). The solder balls on the BGAs can consist of either eutectic solder or high temperature solder (5 % – 10 % Sn) whereas the solder columns on the CGAs always consist of high temperature solder. Although BGAs are usually presented as a device family, there exist a large number of BGA devices with wide-ranging properties. The vast majority of BGA devices are non-hermetic.	
Device with Inward formed L-shaped leads e.g. moulded tantalum chip capacitors.	
Device with flat lug leads This package has flat leads extending from the sides.	
Leaded device with thermal plane termination e.g. Diode PAcKage (DPAK).	  DPAK
Leadless device with thermal plane termination This SMD package consists of three terminal pads, ceramic housing, and lid brazed together to form a hermetic semiconductor die carrier.	

Contents

Figures

Tables

(This page is intentionally left blank)

1

Scope

This Standard defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits based on surface mounted device (SMD) and mixed technology.

The Standard defines acceptance and rejection criteria for high-reliability manufacture of surface-mount and mixed-technology circuit assemblies intended to withstanding normal terrestrial conditions and the vibrational g-loads and environment imposed by space flight.

The proper tools, correct materials, design and workmanship are covered by this document. Workmanship standards are included to permit discrimination between proper and improper work.

The assembly of leaded devices to through-hole terminations and general soldering principles are covered in ECSS-Q-70-08.

Requirements related to printed circuit boards are contained in ECSS-Q-70-10 and ECSS-Q-70-11. The substrates covered by this document are divided into five classes in accordance with their average X and Y coefficient of thermal expansion (CTE).

The mounting and supporting of components, terminals and conductors prescribed herein applies to assemblies designed to operate within the temperature limits of -55 °C to +85 °C.

For temperatures outside this normal range, special design, verification and qualification testing is performed to ensure the necessary environmental survival capability.

Special thermal heat sinks are applied to devices having high thermal dissipation (e.g. junction temperatures of 110 °C, power transistors) in order to ensure that solder joints do not exceed 85 °C.

Verification of SMD assembly processes is made on test vehicles (surface mount verification samples). Temperature cycling ensures the operational lifetime for spacecraft. However, mechanical testing only indicates SMD reliability as it is unlikely that the test vehicle represents every flight configuration.

Examples of the method for achieving SMD verification approval and guidelines for the soldering of area array devices are given in the Annexes.

This Standard does not cover the qualification and acceptance of the EQM and FM equipment with surface-mount and mixed-technology.

The qualification and acceptance tests of equipment manufactured in accordance with this Standard are covered by ECSS-E-10-03.

(This page is intentionally left blank)

2

Normative references

The following normative documents contain provisions which, through references in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-P-001B	ECSS — Glossary of terms
ECSS-M-50B	Space project management — Information/documentation management
ECSS-Q-20B	Space product assurance — Quality assurance
ECSS-Q-20-09B	Space product assurance — Nonconformance control system
ECSS-Q-60B	Space product assurance — Electrical, electronic and electromechanical (EEE) components
ECSS-Q-60-05A	Space product assurance — Generic procurement requirements for hybrid microcircuits
ECSS-Q-70B	Space product assurance — Materials, mechanical parts and processes
ECSS-Q-70-01A	Space product assurance — Cleanliness and contamination control
ECSS-Q-70-02A	Space product assurance — A thermal vacuum outgassing test for the screening of space materials
ECSS-Q-70-08A	Space product assurance — The manual soldering of high–reliability electrical connections
ECSS-Q-70-10A	Space product assurance — Qualification of printed circuit boards
ECSS-Q-70-11A	Space product assurance — Procurement of printed circuit boards
ECSS-Q-70-71A	Space product assurance — Data for selection of space materials
MIL-STD-883 Method 2009.8	

(This page is intentionally left blank)

3

Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ECSS-P-001 and the following apply.

3.1.1
approval authority
entity that reviews and accepts the verification programme, evaluating the test results and grants the final approval

3.1.2
co-planarity
maximum distance between lowest and highest termination when device rests on flat surface

3.1.3
electrical clearance
spacing between non-common electrical conductors on external layers of a printed circuit board assembly

NOTE The distance between conductors depends on the design voltage and DC or AC peaks. Any violation of minimum electrical clearance as a result of a nonconformance is a defect condition.

3.1.4
scavenging (leaching)
basis metal or metallization partly or wholly dissolved in melted solder during a soldering operation

3.1.5
selective plating
tin–lead plated solder pads connected to gold plated copper tracks

NOTE It is usually related to RF circuits

3.1.6
solder balling (solder balls)
numerous spheres of solder having not melted in with the joint form and being scattered around the joint area normally attached by flux residues

NOTE Can be caused by incorrect preheating or poor quality solder.

3.1.7
tombstoning
chip components lifting off one of their two terminal pads causing the chip to stand up like a tombstone.

NOTE Normally caused by:

- bad design where one pad reaches solder reflow temperature before the other;
- different quantities of solder paste on each pad;
- different solderability of one pad or one termination with respect to the other.

3.1.8
underfill
encapsulant material deposited between a device and substrate used to reduce the mechanical stress resulting from a mismatch in the coefficient of thermal expansion (CTE) between the device and the substrate

3.1.9
dynamic wave soldering machine
system that achieves wave soldering and which consists of stations for fluxing, preheating, and soldering by means of a conveyer

3.2 Abbreviated terms

The following abbreviated terms are defined and used within this document:

Abbreviation	Meaning
BGA	ball grid array
CBGA	ceramic ball grid array
CGA	column grid array
CCGA	ceramic column grid array
CLCC	ceramic leaded chip carrier
CTE	coefficient of thermal expansion
JEDEC	Joint Electron Device Engineering Council
LCCC	leadless ceramic chip carrier
MELF	metal electrode face bonded NOTE Also known as minimelf or micromelf
MCGA	multichip column grid array
PCB	printed circuit board
PLCC	plastic leaded chip carrier
PID	process identification document
QFP	quad flat pack
r.m.s.	root–mean–square
SMD	surface mounted device
SMT	surface-mount technology
SO	small outline
SOD	small outline device
SOT	small outline transistor
TO	transistor outline

4

Principles of reliable soldered connections

The following are the general principles to ensure reliable soldered connections:

- Reliable soldered connections are the result of proper design, control of tools, materials, processes and work environments, and workmanship performed in accordance to verified and approved procedures, inspection control and precautions.
- The basic design concepts to ensure reliable connections and to avoid solder joint failure are as follows:
  - Stress relief is an inherent part of the design, which reduces detrimental thermal and mechanical stresses on the solder connections.
  - Where adequate stress relief is not possible materials are so selected that the mismatch of thermal expansion coefficients is a minimum at the constraint points in the device mounting configuration.
- The assembled substrates are designed to allow easy inspection.
- Since only the outer row of solder joints to area array packages can be visually inspected, inner rows are inspected using X-ray techniques. To facilitate X-ray inspection of the solder joints to BGAs, the solder pads have a teardrop design.
- Circuit designs for area array devices, (e.g. BGA, CGA) have clearance around the perimeter of these packages to ensure that reflow nozzles can perform rework or repair operations (see ECSS-Q-70-28 [12]). The clearance depends on the equipment used for reworking and the height of adjacent components.

  NOTE Unpopulated areas on the underside of the substrate assist indirect heating for removal of these packages. See also Annex C, subclause C.3.
- Soldering to gold using tin-lead alloy can cause failure.

(This page is intentionally left blank)

5

Process identification document (PID)

5.1 General

5.1.1 Purpose

The purpose of the PID is to ensure that a precise reference is established for the assembly processes approved in accordance with this Standard.

The PID provides a standard reference against which any anomalies occurring after the approval can be examined and resolved.

5.1.2 Document preparation

The supplier shall prepare the PID according to subclause 5.1.3.

5.1.3 Content

a. The PID shall comprise
   (a) the assembly design configuration
   (b) materials and components used in manufacture
   (c) all manufacturing assembly processes and production controls
   (d) all inspection steps with associated methods.

   NOTE This ensures that all future assemblies supplied by the manufacturer are manufactured according to procedures that are identical to those for which approval was granted.

b. All processes and procedures shall be verified and approved.

5.1.4 Approval

a. The PID shall be submitted to the approval authority

b. The Approval authority shall approve the PID.

5.2 Production control

a. The PID shall contain a production flow chart which identifies all individual processes, inspections and a summary table that compiles all verified surface mount components and materials

   NOTE See Annex B for examples.

b. The points of application of quality controls shall be identified.

c. The flow chart shall present the processes, inspections and quality controls schematically in their correct sequence and, for each operation, make reference to the corresponding documents.

d. The issue number and date of documents applicable at the time of preparation of the flow chart shall be stated.

e. The following symbols shall be used to prepare the chart:

for process and assembly operations

for inspection and test operations

for quality control operations

5.3 Process identification document updating

a. The PID shall be managed in accordance with ECSS-M-50.

b. A PID shall represent the current verified manufacturing processes and production controls.

c. Any proposed changes to the PID shall be agreed by the Approval authority.

d. The supplier shall identify the need for additional testing to be approved by the Approval authority.

e. The PID, the summary table and the relevant applicable documents shall be re-issued and agreed by the Approval authority.

6

Preparatory conditions

6.1 Calibration

Records of tool calibration and verification shall be maintained.

6.2 Facility cleanliness

ECSS-Q-70-08A, subclause 5.1 shall apply.

6.3 Environmental conditions

ECSS-Q-70-08A, subclause 5.2 shall apply.

6.4 Precautions against static charges

ECSS-Q-70-08A,subclause 5.3 shall apply.

6.5 Lighting requirements

ECSS-Q-70-08A, subclause 5.4 shall apply.

6.6 Equipment and tools

6.6.1 Brushes

ECSS-Q-70-08A, subclause 5.5.1 shall apply.

6.6.2 Pliers

ECSS-Q-70-08A, subclause 5.5.2 shall apply.

6.6.3 Bending tools

ECSS-Q-70-08A, subclause 5.5.4 shall apply.

6.6.4 Clinching tools

ECSS-Q-70-08A, subclause 5.5.5 shall apply.

6.6.5 Insulation strippers

ECSS-Q-70-08A, subclause shall 5.5.6 apply.

6.6.6 Soldering tools

ECSS-Q-70-08A, subclause 5.5.9 shall apply.

6.6.7 Soldering irons and resistance soldering equipment

a. ECSS-Q-70-08A, subclause 5.5.7 shall apply.

b. For surface mounted devices, the soldering tip shall not exceed 340 °C.

NOTE Based on the component manufacturer's recommendations, solder iron can be substituted by applying, for instance, hot air in order to avoid thermal shock.

6.6.8 Non–contact heat sources

ECSS-Q-70-08A, subclause 5.5.8 shall apply.

6.6.9 Solder pots and baths

ECSS-Q-70-08A, subclause 7.1.6 shall apply.

6.7 Soldering machines and equipment

6.7.1 General

a. Machines and equipment used to solder surface mount devices:

1. leadless and leaded devices specifically designed for surface mounting,
2. components initially designed for insertion mounting,

shall either be a type incorporating dynamic single or dual solder wave, or be of the solder reflow type.

b. The soldering machine shall be grounded in order to avoid electrostatic discharge.

c. The supplier shall ensure that the soldering conditions do not exceed the values given by the individual component data sheets (e.g. maximum temperature to avoid internal melting, removal of marking ink, degradation of encapsulating plastic).

d. Temperature and time profiles for assembly shall be identified by the supplier and approved by the approval authority.

6.7.2 Dynamic wave-solder machines

Dynamic soldering machines shall be of automatic type and of a design offering the following:

a. Controllable preheating to drive off volatile solvents and to avoid thermal shock damage to the PCB and component packages.

b. The capacity to maintain the solder temperature at the printed circuit board assembly to within 5 °C of the established bath temperature throughout the duration of any continuous soldering run when measured 3,0 mm below the surface of the wave.

c. A wave system that limits shadowing and allows solder fillet formation.

d. Carriers made from a material that cannot contaminate, degrade or damage the printed circuit board or substrate nor transmit vibrations or shock stress from the conveyors to a degree permitting physical, functional or electrostatic damage to devices, board or substrate during transport through preheating, soldering and cooling stages.

e. An extraction system, either integral or separate, conforming to the requirements of subclauses 6.2 and 6.3.

6.7.3 Condensation (vapour phase) reflow machines

Condensation reflow machines shall conform to the following requirements:

a. Not transmit a movement or vibration into the assemblies being soldered that result in misalignment of parts or disturbed solder joints.

b. Be capable of preheating an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

c. Use a reflow fluid whose boiling point is a minimum of 12 °C above the melting point of the solder being used.

d. Maintain the preselected temperature to within ±5 °C in the reflow zone during soldering.

e. Include an extraction system that conforms to subclauses 6.2 and 6.3.

6.7.4 Hot gas reflow machines

Hot gas reflow machines shall conform to the following requirements:

a. Does not transmit movement or vibration to the assemblies being soldered which result in misalignment of parts or disturbed solder joints.

b. Preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

c. Heats the area of the assembly to be soldered to a preselected temperature between 220 °C and 250 °C as measured on the substrate surface.

d. Prevents the reflow of adjacent components.

e. Maintains the preselected reflow temperature within ±5 °C as measured at the substrate surface.

6.7.5 Shorted bar and parallel gap resistance reflow machines

Resistance reflow machines shall be of a design such that the system meets the following requirements:

a. Does not impart mechanical damage to the component leads.

b. Provides “time at temperature” control type of power supply.

c. Maintains the shorted bar or component lead to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used.

d. Maintains the dwell time at temperature to within 5 % of the preset value.

e. Provides a repeatable down force to within 15 % of the preset value.

f. Provides a system (e.g. an optical feature) to ensure that the shorted bar or electrode alignment with the component lead foot is within 20 % of the nominal lead foot length.

6.7.6 Convection and radiation reflow systems

Convection and radiation reflow machines shall be of design such that the system meets the following requirements:

a. Provides a controlled temperature profile and does not transmit movement or vibration into the assembly being soldered.

b. Preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

c. Heats the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used as measured at laminate or substrate surface.

d. Maintains the preselected temperature to within 6 °C in the reflow zone during soldering.

6.7.7 Other equipment for reflow soldering

Other solder reflow systems can be approved for use by the Approval authority. This approval shall be subject to compliance with subclauses 6.7.1 to 6.7.6.

6.8 Ancillary equipment

6.8.1 General

Equipment shall not generate, induce or transmit electrostatic charges to devices being placed.

6.8.2 Solder deposition equipment

a. Equipment used to deposit solder pastes shall be of a screening, stencilling, dispensing, roller coating or dotting type.

b. Equipment shall apply pastes of a viscosity and quantity such that the positioned device is retained on the board before and during soldering operations, ensuring self-centring and solder fillet formation.

c. Equipment used to apply solder preforms shall ensure alignment of the preform with the land or device lead and termination.

6.8.3 Automatic device placement equipment

a. Automatic or computer controlled equipment used for device placement shall be of the coordinate-driven pick-and-place type or of the robotic type.

b. The placement equipment used shall be of a type that:

1. prevents device or board damages
2. indexes devices with respect to the circuit
3. aligns the device leads or castellations with the board terminal areas.

6.8.4 Cleaning equipment and systems

ECSS-Q-70-08A, subclauses 11.1 and 11.2 shall apply.

6.8.5 Cleanliness testing equipment

ECSS-Q-70-08A, subclause 11.3.1 shall apply.

6.8.6 Magnification aids

Subclause 13.1 shall apply.

6.8.7 X-ray inspection equipment

a. X-ray inspection shall not damage the components.

b. X-ray equipment shall be calibrated in order to evaluate the total dose received by the components during the inspection.

NOTE In order to minimize the dose given to the component, it is good practice to:

- Record the total dose received.
- Use off-line image analysis as much as possible.
- Use filters, optimizing the direction of the X-ray beam and masking sensitive areas.

c. The resolution of the X-ray equipment shall be able to detect solder balls having a diameter of 0,03 mm.

d. The sensitivity shall be demonstrated by means of actual 0,03 mm diameter solder balls, stuck to adhesive tape, attached to the multilayer board assembly being inspected.

NOTE For guidelines, see C.4.3 and E.1 for X-ray inspection.

6.8.8 Metallographic equipment

The metallographic equipment shall enable mounting, cross-sectioning and polishing of the solder interconnections.

(This page is intentionally left blank)

7

Material selection

7.1 General

Material selection shall be performed in accordance with ECSS-Q-70-71.

7.2 Solder

7.2.1 Form

a. Solder paste, ribbon, wire and preforms shall be used provided that the alloy and flux meet the requirements in subclause 7.2.2.

b. Alloy for use in solder baths shall be supplied as ingots (without flux).

7.2.2 Composition

a. The solder alloy shall have a composition specified in Table 1, unless approved by the Approval authority.

NOTE 1 See ISO 9453 for further details.

NOTE 2 The solder alloy used depends upon the application. See Annex E.2 for Guide for choice of solder type.

7.2.3 Solder paste

a. Solder paste shall conform to the requirements of subclause 7.2.1.

NOTE The solder ball size and flux percentage are selected depending on the process employed, i.e. screen, stencil or needle application.

b. The metal purity shall be as specified in Table 1.

Table 1: Chemical composition of spacecraft solders

ESA designation	Sn min % - max %	Pb max %	In min % - max %	Sb max %	Ag min % - max %	Bi max %	Cu max %	Fe max %	Zn max %	Al max %	As max %	Cd max %	Other max %
63 tin solder	62,5-63,5	remain	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
62 tin silver loaded	61,5-62,5	remain	-	0,05	1,8-2,2	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
60 tin solder	59,5-61,5	remain	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
96 tin solder	remain	0,10	-	0,05	3,5-4,0	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
75 indium lead	max. 0,25	remain	74,0-76,0	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
70 indium lead	0,00-0,10	remain	69,3-70,7	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
50 indium lead	0,00-0,10	remain	49,5-50,5	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
10 tin lead	9,0-10,5	remain	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08

7.2.4 Maintenance of paste purity

a. When purchased premixed or mixed in house, the purity of solder paste shall be maintained.

b. Manufacturers' instructions shall be applied for the handling and storage of containers of solder paste purchased premixed.

c. Refrigerated solder paste shall reach room temperature before opening the container.

d. Neither paste purchased premixed nor paste mixed in-house shall be used if the use-by date or shelf life recommended by the manufacturer of the paste or paste constituents has expired.

e. When the solder paste's shelf life has expired (see ECSS-Q-70-22 [11]), it shall not be used unless:

   1. relifing is performed
   2. tests that include visual inspection and viscosity measurements (according to the manufacturer's recommendations) are passed successfully.

f. When relifing is performed, and the material passes the specified tests, the new shelf life shall be half the initial shelf life.

g. Tools used for removing solder paste from the container shall not contaminate the paste dispensed or that remaining within.

7.3 Flux

7.3.1 Rosin based flux

ECSS-Q-70-08A, subclause 6.2.1 shall apply.

7.3.2 Corrosive acid flux

ECSS-Q-70-08A, subclause 6.2.2 shall apply.

7.3.3 Flux controls for wave-soldering equipment

A controlled method shall be established and implemented for wave-soldering machines such that the flux is not contaminated with remaining residues from previous non-space works.

7.4 Solvents

7.4.1 Acceptable solvents

ECSS-Q-70-08A, subclause 6.3.1 shall apply.

7.4.2 Drying

ECSS-Q-70-08A, subclause 6.3.2 shall apply.

7.5 Flexible insulation materials

ECSS-Q-70-08A, subclause 6.4 shall apply.

7.6 Terminals

ECSS-Q-70-08A, subclause 6.5 shall apply.

7.7 Wires

ECSS-Q-70-08A, subclause 6.6 shall apply.

7.8 Printed circuit substrates

7.8.1 Selection

a. Printed circuit boards and substrates shall be selected from the classes given in Table 2.

b. The class of board selected shall have a CTE characteristic compatible with the CTE of the devices.

NOTE 1 The objective is that the impact of stresses from the environment is minimized.

NOTE 2 The warp and twist of multilayer boards can affect the geometry of the solder joints.

c. The warp and twist of the printed circuit multilayer board shall be in accordance with ECSS-Q-70-11.

NOTE Symmetrical board design reduces warp and twist of the printed circuit board.

Table 2: Guide for choice of printed circuit boards and substrates

Class	Description	CTE (10^{-6}/°C)
1	Non-compensated printed board	14 - 17
2	Ceramic	5 - 7
3	Compensated printed board	11 - 13
4	Compensated printed board	9 - 11
5	Compensated printed board	5 - 9

7.8.2 Class 1 - Non-compensated printed circuit board

Boards shall be made of materials and manufactured according to the requirements of ECSS-Q-70-10 and procured to ECSS-Q-70-11.

NOTE Typical substrates are epoxy-woven glass and polyimide-woven glass.

7.8.3 Class 2 - Ceramic substrates

Hybrid microcircuits shall meet the requirements of ECSS-Q-60-05.

NOTE Typical PCB ceramic substrates are alumina and aluminium nitride.

7.8.4 Class 3 - Compensated printed circuit board

Boards shall be made of materials and manufactured according to the requirements of ECSS-Q-70-10 and procured according to ECSS-Q-70-11.

NOTE These boards can be reinforced with low CTE fibres such as aramid, quartz or carbon.

7.8.5 Class 4 - Compensated printed circuit board

Boards shall be made of materials and manufactured according to the requirements of ECSS-Q-70-10 and procured according to ECSS-Q-70-11.

NOTE CTE compensated boards use standard construction and are compensated with materials such as a distributed plane consisting of a low CTE material.

7.8.6 Class 5 - Compensated printed circuit board

Boards shall be made of materials and manufactured according to the requirements of ECSS-Q-70-10 and procured according to ECSS-Q-70-11.

NOTE CTE compensated boards use a standard construction with compensated materials such as low CTE substrate or cores. Typical cores are copper-plated invar and copper-plated molybdenum.

7.9 Components

7.9.1 General

a. Components and their finishes shall be selected from those approved according to ECSS-Q-60B, subclause 4.2 and 4.3.

b. Device leads and terminations shall be solder coated with a tin/lead alloy in accordance with Table E-1.

NOTE It is good practice to select the device with solder finish applied over sintered metal on ceramic terminations having a diffusion barrier (nickel or equivalient diffusion layer) layer between the metallization and the solder finish.

c. Solder may be applied to the leads by hot dipping or by plating from a solution.

d. Plated solder terminations shall be subjected to a post plating reflow operation to fuse the solder.

e. The incoming inspection of each component batch shall include the verification of the termination composition (to avoid assembly of pure tin finish).

f. Pure tin finish with more than 97 % purity shall not be used.

NOTE This is due to the possibility of whisker growth and transformation to grey tin powder at low temperatures.

g. Where condensation reflow (vapour phase) is used for assembly, devices shall be capable of withstanding three cycles through the reflow system at its operating temperature (e.g. 215 °C), each cycle consisting of a minimum of 60 seconds of exposure.

h. Where wave soldering is used for surface-mount soldering, devices shall be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C.

i. Devices shall be capable of withstanding cleaning processes currently used in space projects.

7.9.2 Active components

a. Active leadless devices (e.g. transistors, thyristors, diodes, and integrated circuit devices) shall be of a configuration incorporating sintered metal-on-ceramic terminations, solid-reflow termination pads integrated to the device body.

b. Axial leads, wire or ribbon non-axial leads shall be hermetically sealed.

c. Castellated chip carrier components shall have no discontinuities in the metallized terminal areas on the mounting pattern of the device.

7.9.3 Moisture sensitive components

a. Moisture sensitive components shall be stored and handled according to the component manufacturer's recommendations. See also subclause 8.5. b.

NOTE Many types of plastic encapsulated components, particularly some plastic BGAs, are moisture sensitive.

b. When moisture sensitive components are used, bakeout shall be performed in accordance with subclause 8.5 b.

7.9.4 Passive components

a. If passive components initially designed for insertion-mount application are used for surface mounting, they shall be of a style that can be surface-mount adapted to provide conformance with the requirements of subclause 7.9.1.

b. The adaptation as in 7.9.4 a. shall not functionally or physically degrade the component or the substrate to which the adapted component is to be attached.

c. End-capped and end-metallized devices shall have no discontinuities in the terminal areas.

d. The body of the devices shall not be cracked, scored, chipped, broken or otherwise damaged to an extent greater than specified in the applicable procurement specification.

e. Connectors shall be of a configuration incorporating either male or female quick-disconnect contacts and stress relief provision for the soldered connection of each individual contact when such connections are completed.

7.10 Adhesives (staking compounds and heat sinking), encapsulants and conformal coatings

a. Adhesives shall be dispensable, non-stringing, and shall have a reproducible dot profile after application.

b. Adhesives, encapsulant and conformal coating shall be non-corrosive to devices and substrates.

c. The uncured strength shall be capable of holding devices during handling prior to curing.

d. Adhesives, encapsulants and conformal coatings shall conform to the outgassing requirements of ECSS-Q-70-02A, clause 7.

e. Adhesives, encapsulants and conformal coatings shall have no adverse effects upon materials used on the substrate, or devices attached thereon.

NOTE The effects of some conformal coatings on the reliability of mounted SMDs are described in ESA SP-1173 [3].

f. Adhesives, encapsulants and conformal coatings shall be selected based on their thermal conductivity and dielectric properties (see ESA STM 265 [2]).

NOTE Some thermally conductive adhesives used to dissipate Joule heating are listed in ESA STM-265 "Evaluation of Thermally

Conductive Adhesives as Staking Compounds during the Assembly of Spacecraft Electronics" [2].

g. The capability of the adhesives to meet their requirements shall be demonstrated by means of a verification test programme according to clause 14.

NOTE Adhesion to fused tin/lead finishes is poor (see also ECSS-Q-70-28).

h. Stress relief of device leads shall not be negated by the encapsulants or conformal coatings.

NOTE 1 This is particularly important at low service temperatures.

NOTE 2 The coefficient of expansion, glass transition temperature and modulus of adhesives used under devices for thermal reasons, for achieving stand-off heights or mechanical support during vibration, can be considered to ensure that the additional stress put on the solder joints does not degrade the solder joint reliability.

8

Preparation for soldering

8.1 Preparation of devices and terminals

8.1.1 Preparation of wires and terminals

ECSS-Q-70-08A, subclause 7.1 shall apply.

8.1.2 Preparation of surfaces to be soldered

ECSS-Q-70-08A, subclause 7.1.5 shall apply.

8.1.3 Degolding and pretinning of conductors

ECSS-Q-70-08A, subclause 7.1.6 shall apply.

8.1.4 Alloying of pure tin finish

Tin finish with more than 97 % tin purity shall not be used.

NOTE 1 This is due to the possibility of whisker growth and transformation to grey tin powder at low temperature.

NOTE 2 Pure tin terminations can be dipped into liquid solder as described in ECSS-Q-70-08A, subclause 7.1.6 in order to replace the tin with tin-lead alloy.

8.2 Preparation of solder bit

ECSS-Q-70-08A, subclause 7.2 shall apply.

8.3 Handling

ECSS-Q-70-08A, subclause 7.4 shall apply.

8.4 Storage

ECSS-Q-70-08A, subclause 7.5 shall apply.

8.5 Baking of PCBs and moisture sensitive components

a. ECSS-Q-70-08A, subclause 7.6 shall apply for PCBs, partially assembled PCBs and assemblies going through reworking.

b. Baking of moisture sensitive devices before an assembly process shall be implemented.

NOTE This is to counteract the “popcorn” effect in soldering using oven or vapour phase reflow techniques.

c. Baking times and temperatures shall be documented.

NOTE 1 Typical baking conditions are from 6 h to 24 h at 125 °C depending on the JEDEC classification, except for components delivered in reels for which a lower temperature and longer time are used.

NOTE 2 It is good practice to store components under nitrogen, dry air (20 % RH maximum) or partial vacuum.

9

Mounting of devices prior to soldering

9.1 General requirements

ECSS-Q-70-08A, subclause 8.1 shall apply.

9.2 Lead bending and cutting requirements

ECSS-Q-70-08A, subclause 8.2 shall apply.

9.3 Mounting of terminals to PCBs

ECSS-Q-70-08A, subclause 8.3 shall apply.

9.4 Lead attachment to through holes

ECSS-Q-70-08A, subclause 8.4 shall apply.

9.5 Mounting of components to terminals

ECSS-Q-70-08A, subclause 8.5 shall apply.

9.6 Mounting of connectors to PCBs

ECSS-Q-70-08A, subclause 8.7 shall apply.

9.7 Surface mount requirements

9.7.1 General

a. Devices to be mounted shall be designed for, and be capable of withstanding the soldering temperatures of the particular process being used for fabrication of the assembly.

b. Surface mounted devices may be mounted on either one side or both sides of a printed circuit assembly.

c. Devices incapable of withstanding machine soldering temperatures shall be hand soldered in a subsequent operation.

9.7.2 Stress relief

When Class 1 boards are employed (i.e. glass fibre epoxy or glass fibre polyimide resins with no CTE compensation), the supplier shall accommodate CTE mismatch by the mounting technology.

NOTE 1 Pure eutectic tin–lead solder or indium–lead solder provide better stress relief (due to their ductility) than those with additional elements, e.g. antimony, gold.

NOTE 2 Leadless devices with e.g. end-cap terminations, metallizations, can have some stress relief (such as additional foil or wire leads, possibly attached by welding or high melting point solder).

NOTE 3 A solder stand-off (see Figure 2, dimension "X") can assist stress relief; in this situation, the CTE mismatch strain is taken up by the ductile solder.

NOTE 4 CTE compensated substrates or laminates of Classes 2 - 5 (listed in subclause 7.8) can be selected to match the CTE of large leadless packages.

9.7.3 Registration of devices and pads

a. Devices shall be mounted on their associated terminal pads (lands).

b. The spacing between conductive elements shall not be reduced below the minimum electrical spacing specified in ECSS-Q-70-11A, Tables 1, 2, 4 and 5 .

NOTE Some surface mounted components that are not bonded to the PCB can self-align during the soldering process. It is the registration after soldering that is important.

9.7.4 Lead forming

a. The leads of leaded surface mount devices shall be formed to their final configuration prior to mounting.

b. Forming shall not degrade the solderability or cause loss of plating adhesion to the leads.

c. Forming shall not cause mechanical damage to the leads or attachment seals.

d. Leads of dual-in-line and gull-wing packages, flat-packs and other multi-leaded devices shall be dressed (mechanically re-aligned) to ensure co-planarity.

9.7.5 Mounting devices in solder paste

a. Both leaded and leadless surface mounted devices shall be mounted in solder paste prior to reflow soldering.

NOTE It is good practice to optimize the pick and place mounting force on the device lead, ball or column.

b. The solder paste deposited on each solder land shall be visually inspected for registration and coverage by the operator prior to mounting the devices.

NOTE After device mounting, the solder paste can extend beyond the edge of the pad by up to 40 % of the conductor separation.

9.7.6 Leadless devices

a. Devices shall not be stacked.

b. Devices shall not bridge the spacing between other parts or components such as terminals or other properly mounted devices.

c. Except for RF applications, devices with electrical elements deposited on an external surface (such as resistors) shall be mounted with that surface facing away from the printed circuit board or substrate.

NOTE See Figure 1 for details.

d. Devices that are bonded to the PCB prior to wave- or reflow-soldering shall be placed so that the requirements after soldering given in clause 11 are met.

e. The adhesive shall not extend onto the solder pads.

f. Artificial stand-off (e.g. elevation as seen in subclause 11.5.5) may be achieved by removable spacers or other techniques according to fully documented procedures.

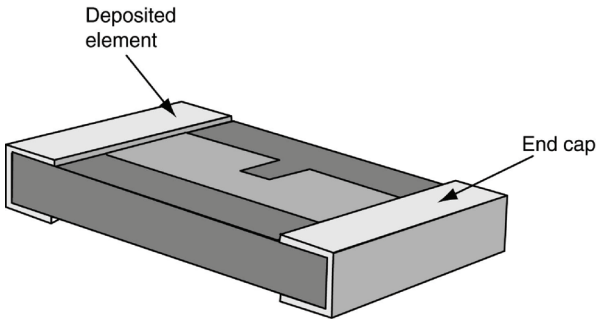


Figure 1: Exposed element

9.7.7 Leaded devices

Surface mounting of leaded (round or flattened cross section) devices shall be parallel to the board surface.

9.7.8 Area array devices

There shall be no more than three reflow operations on a single device

NOTE Any reworking constitutes one reflow operation (see also C.2.5.1).

9.7.9 Staking of heavy devices

a. Staking compounds shall be selected according to subclause 7.10.

b. Contamination shall be removed prior to staking.

NOTE Some surfaces can be prepared to enhance the adhesion (e.g. by mechanical abrasion).

c. Staking compounds shall be mixed and cured in accordance with the manufacturer's procedures.

d. The process of applying the staking compound shall be controlled by a written procedure which defines the location of the staking compound, the volume and the spread area (between device bottom surface and substrate upper surface).

e. The staking compound shall not negate the stress relief of the device, nor come into contact with surrounding devices.

f. All devices except area arrays weighing more than 5 g shall be staked.

NOTE 1 This is to minimize shock and vibration loading on the leads

NOTE 2 The staking compound can be applied either before or after soldering according to the supplier's process identification document.

(This page is intentionally left blank)

10

Attachment of conductors to terminals, solder cups and cables

ECSS-Q-70-08A, clause 9 shall apply.

(This page is intentionally left blank)

11

Soldering to terminals and printed circuit boards

11.1 General

ECSS-Q-70-08A, subclause 10.1 shall apply.

11.2 Solder application to terminals

ECSS-Q-70-08A, subclause 10.2 shall apply.

11.3 Solder applications to PCBs

ECSS-Q-70-08A, subclause 10.3 shall apply.

11.4 Wicking

ECSS-Q-70-08A, subclause 10.4 shall apply.

11.5 Soldering of SMDs

11.5.1 General requirements

a. Devices shall not be mounted on flexible substrates according to ECSS-Q-70-10A, subclause 3.1.6.

b. Soldering to gold with tin/lead alloys shall not be performed (see also subclause 8.1.3).

c. Devices shall not be stacked nor bridge the space between other parts or components (e.g. as terminals or other properly mounted devices).

d. Mispositioning of devices shall not reduce the specified minimum electrical clearance to adjacent tracks or other metallized elements.

e. Non-axial-leaded devices (e.g. small outline, flat-packs and similar devices) shall be mounted with all leads seated on a terminal area to ensure mechanical strength.

f. Solder shall cover and wet the solderable surfaces as specified in subclause 13.2.

11.5.2 End-capped and end-metallized devices

End-capped and end-metallized devices having terminations of a square or rectangular configuration (such as chip resistors, chip capacitors, MELFs and

similar leadless discrete components) can have three or five face terminations, as shown in "a" and "b" in Figure 2.

a. There shall be no discernible discontinuities in the solder coverage of the terminal areas of devices.

b. Solder shall not encase any non-metallized portion of the body of the device following reflow.

c. The solder joints to these devices shall meet the dimensional and solder fillet requirements of Table 3 and Figure 2.

Table 3: Dimensional and solder fillet requirements for rectangular and square end capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum lap contact	L	0,13 mm
Minimum fillet height	M	X + 0,3 × H or X + 0,5 mm whichever is less
Stand-off (elevation)	X	Present up to 0,4 mm
Maximum tilt limit	C	10°
Minimum solder coverage of edges on terminal pad	-	75 % (see Annex E.1)

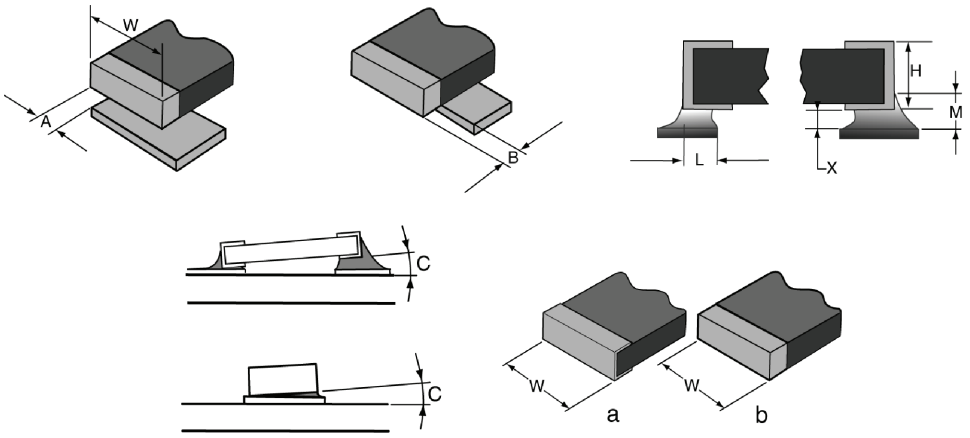


Figure 2: Mounting of rectangular and square end-capped and end-metallized devices

11.5.3 Bottom terminated chip devices

Devices having metallized terminations on the bottom side only (e.g. discrete chip components, ceramic leadless chip carriers) shall meet the dimensional and solder fillet requirements of Table 4 and Figure 3.

Table 4: Dimensional and solder fillet requirements for bottom terminated chip devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum lap contact	L	0,75 × W
Stand-off (elevation)	X	0,1 mm to 0,4 mm

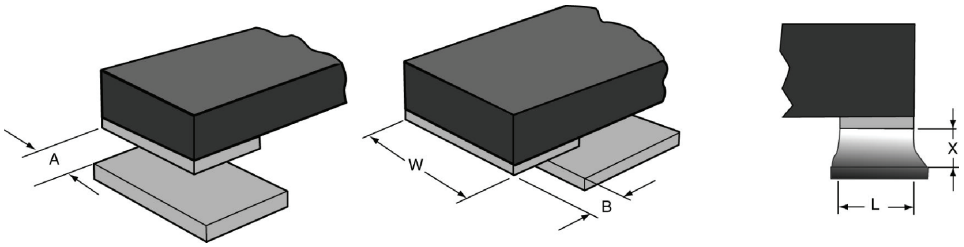


Figure 3: Mounting of bottom terminated chip devices

11.5.4 Cylindrical end-capped devices

Solder joints to components having cylindrical terminations (such as MELF and SOD components) shall meet the dimensional and solder fillet requirements of Table 5 and Figure 4.

Table 5: Dimensional and solder fillet requirements for cylindrical end-capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × D
End overhang	B	Not permitted
Minimum fillet width	E	0,5 × D
Minimum fillet height	M	X + 0,3 × D or X + 1,0 mm whichever is less
Minimum side fillet length	L	0,5 × T
Stand-off (elevation)	X	Present up to 0,75 mm

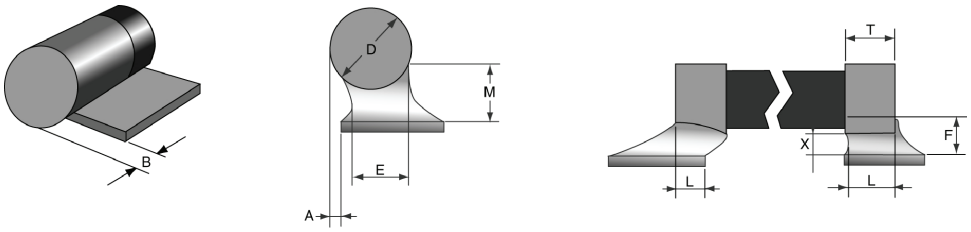


Figure 4: Mounting of cylindrical end-capped devices

11.5.5 Castellated chip carrier devices

Joints to castellated device terminations shall meet the dimensional and solder fillet requirements of Table 6 and Figure 5.

NOTE 1 The stand-off enables adequate cleaning beneath the assembled LCCC and also to enhance solder fatigue life (see also subclause 9.7.6 f.)

NOTE 2 Devices bigger than LCCC 16 are not expected to be used for space applications when mounted on Class 1 substrates.

Table 6: Dimensional and solder fillet requirements for castellated chip carrier devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Zero
Maximum fillet length	E	P
Minimum fillet height	M	0,25 × H
Stand-off (elevation)	X	0,1 mm to 0,4 mm

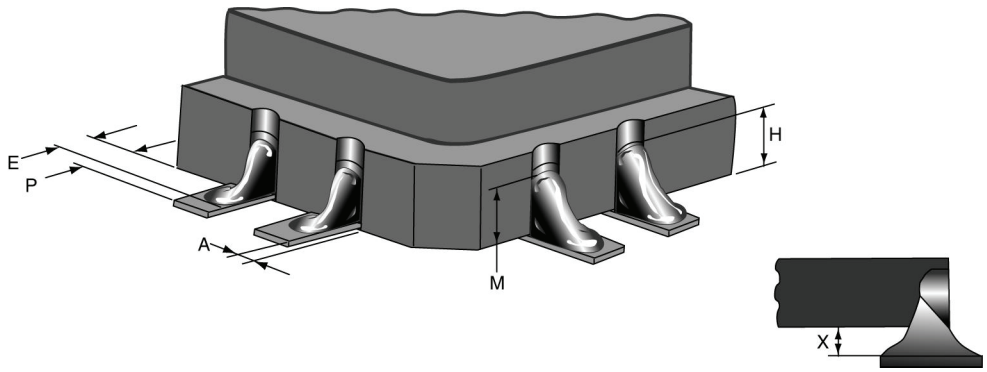


Figure 5: Mounting of castellated chip carrier devices

11.5.6 Devices with round, flattened, ribbon, "L" and gull-wing leads

Solder joints formed to round, flattened, ribbon, "L" and gull-wing shaped leads shall meet the dimensional and solder fillet requirements of Table 7 and Figure 6.

Table 7: Dimensional and solder fillet requirements for devices with round, flattened, ribbon, "L" and gull-wing leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to pad edge at toe	B	0,20 mm
Minimum distance to pad edge at heel	L	0,5 × W
Minimum side joint length	D	1,5 × W
Minimum heel fillet height	E	X + T

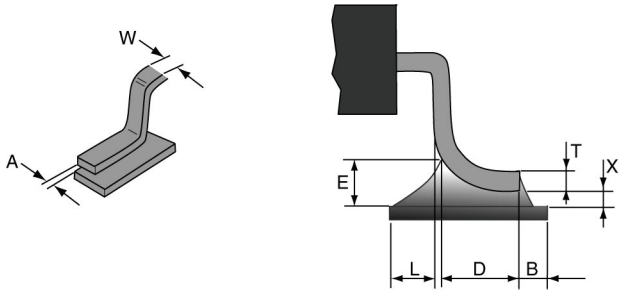


Figure 6: Mounting of devices with round, flattened, ribbon, "L" and gull-wing leads

11.5.7 Devices with "J" leads

Solder joints formed to "J" and "V" shaped leads shall meet the dimensional and solder fillet requirements of Table 8 and Figure 7.

Table 8: Dimensional and solder fillet requirements for devices with "J" leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum side joint length	L	1,5 × W
Minimum heel fillet height	M	X + T
Maximum stand-off	X	0,75 mm

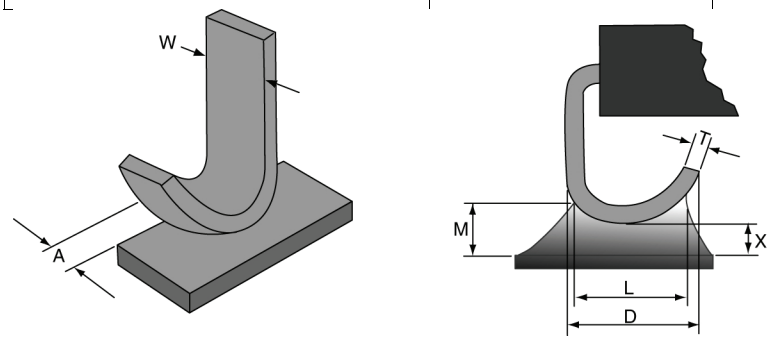


Figure 7: Mounting of devices with "J" leads

11.5.8 Area array devices

a. The outer row of solder joints to area array devices shall be visually inspected by looking from the side in accordance with the requirements in 11.5.1 and Table 9 and with the rejection criteria specified in 13.3 and 13.4.

b. Inner rows of solder joints shall be inspected using X-ray techniques in accordance with subclause 6.8.7 and Table 9.

NOTE 1 Annex C, subclause C.4.3 and the workmanship standard shown in subclauses 16.2 and 16.3 can be used as guidelines for such an inspection.

NOTE 2 As it is impossible to visually inspect solder joints to area array devices, reliability of these devices cannot be assured by inspection and rework. Even using X-ray techniques, some types of defect are difficult to detect. Therefore, reliability of these solder joints can only be assured by robust process control. Quality assurance guidance for these types of devices is given in Annex C.

NOTE 3 Examples of typical area array devices are shown in Figures 8, 9 and 10.

Table 9: Dimensional and solder fillet requirements for area array devices

Parameter	Dimension limits
Misplacement	0,15 × D (for outer edge)
BGA ball	Collapse of BGA ball spacing does not violate minimum electrical clearance or become less than 0,10 mm.
Maximum component height	Overall height of component does not exceed maximum specified.
Soldered connection	a. BGA balls contact and wet to the land forming a continuous elliptical connection consistent with the tear drop. b. CGA solder columns contact and wet to the land forming a continuous connection
Voids in the solder region (see C.2.2)	Voids to the solder-to-package interface or solder-to-PCB interface: a. max. 25 % of the BGA ball cross section. b. max. 25 % of the column cross section diameter, by X-ray or microsection or alternative technique.
Solder balls	Any solder ball having a diameter greater than 0,1 mm shall be rejected. The total number of solder balls having a diameter greater than 0,03 mm shall not exceed 10 per device.
Maximum CGA column tilt	5 degrees
D = pad diameter (not including any teardrop extension)	

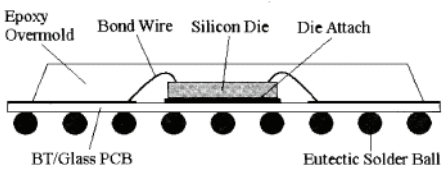


Figure 8: Typical plastic ball grid array (PBGA)

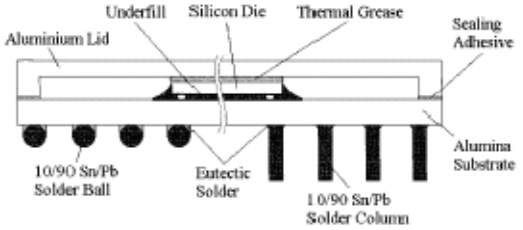


Figure 9: Typical ceramic area array showing ball grid array configuration on left and column grid array on right (CBGA & CCGA)

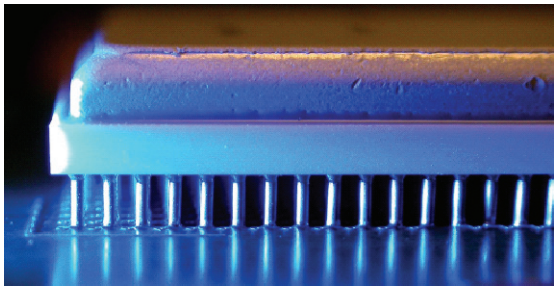


Figure 10: Typical assembled CCGA device

11.6 Tall profile devices

a. Tall profile components having bottom only terminations, as illustrated in Figure 11, shall not be used if the height (V) is greater than the width or breadth (T).

b. Devices taller than 12 mm in height shall be bonded or secured to the board without reducing the existing lead stress relief.

NOTE This is to minimize shock and vibration loading on the part leads

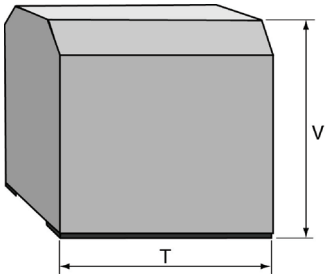


Figure 11: Dimensions of tall profile components

11.7 Staking of solder assembly

When devices, except area arrays, weighing more than 5 g are not staked or secured to the board prior to soldering, they shall be staked or secured after soldering according to subclause 9.7.9.

11.8 Underfill

Underfill beneath area arrays may be applied if it does not restrict the possibility of device removal.

NOTE 1 For power dissipation thermal adhesive can be used provided that it does not contravene the requirement of this standard (see ESA STM-265 for suitable silicone product) [2].

NOTE 2 Underfill has been observed to promote thermal fatigue of soldered connections during thermal cycling (see ESA STM-266 [4]).

12

Cleaning of PCB assemblies

12.1 General

ECSS-Q-70-08A, subclause 11.1 shall apply.

12.2 Ultrasonic cleaning

ECSS-Q-70-08A, subclause 11.2 shall apply.

12.3 Monitoring for cleanliness

ECSS-Q-70-08A, subclause 11.3 shall apply.

(This page is intentionally left blank)

13

Final inspection

13.1 General

a. Each soldered connection shall be visually inspected in accordance with the criteria specified in the subclauses below.

b. Inspection shall be aided by magnification appropriate to the size of the connections between 4X and 10X.

c. Additional magnification shall be used to resolve suspected anomalies or defects.

d. Parts and conductors shall not be physically moved to aid inspection.

e. The substrate, components and component position, as well as the fasteners and the mounting hardware, shall be inspected in accordance with the requirements in subclause 11.5.

NOTE Clause 16 includes examples of acceptable and unacceptable workmanship.

13.2 Acceptance criteria

Acceptable solder connections shall be characterised by:

a. clean, smooth, satin to bright undisturbed surface,

b. solder fillets between conductor and termination areas as described and illustrated in clause 16,

c. visible contour of wires and leads such that their presence, direction of bend and termination end can be determined,

d. complete wetting as evidenced by a low contact angle between the solder and the joined surfaces,

e. acceptable amount and distribution of solder in accordance with subclause 11.5,

f. absence of any of the defects mentioned in subclauses 13.3 and 13.4.

13.3 Visual rejection criteria

The following are some characteristics of unsatisfactory conditions, any of which shall be cause for rejection:

a. charred, burned or melted insulation of parts,

b. conductor pattern separation from circuit board,
c. burns on base materials,
d. continuous discolouration between two conductor patterns (e.g. measling, delamination, halo effect),
e. excessive solder (including peaks, icicles and bridging), see clause 16,
f. flux residue, solder splatter, solder balls, or other foreign matter on circuitry, beneath components or on adjacent areas,
g. dewetting,
h. insufficient solder, see clause 16,
i. pits, holes or voids, or exposed base metal (excluding the ends of cut leads) in the soldered connection,
j. granular or disturbed solder joints,
k. fractured or cracked solder connection,
l. cut, nicked, gouged or scraped conductors or conductor pattern,
m. incorrect conductor length,
n. incorrect direction of clinch or lap termination on a PCB
o. damaged conductor pattern,
p. bare copper or base metal, excluding the ends of cut wire or leads or sides of tracks and soldering pads on substrate,
q. soldered joints made directly to gold-plated terminals or gold-plated conductors using tin-lead solders,
r. cold solder joints,
s. component body embedded within solder fillet,
t. open solder joints (e.g. tombstoning),
u. probe marks present on the metallization of chip devices caused by electrical testing after assembly.
v. Glass seal does not conform to MIL-STD-883 Method 2009.8.

13.4 X-ray rejection criteria for area array devices

The following are some characteristics of not acceptable conditions from X-ray inspection, utilizing equipment defined in subclause 6.8.7, any of which shall be cause for rejection:

a. criteria and dimensions outside the limits given in Table 9,
b. bridges,
c. for BGA: non-wetting of the solder on the teardrop pad.

13.5 Warp and twist of populated boards

Warp and twist exceeding the requirement of ECSS-Q-70-11A Table 1, 4 and 5, shall not be reduced after solder operation.

NOTE Shims can be used to accommodate warp and twist during integration.

13.6 Inspection records

The result of the final inspection shall be recorded on the shop traveller.

14

Verification procedure

14.1 General

a. The supplier shall establish a verification programme to be approved by the Approval authority.

NOTE Annex A presents an example of such a programme

b. The supplier shall demonstrate verification for each combination of substrate class, SMD type, soldering technique applied, staking compound and conformal coating as used on flight models.

c. Both, the verification of the assembly by hand and machine soldering shall be made in accordance with this clause 14.

d. The supplier shall design surface mount verification samples (test vehicles) using printed circuit board substrates (e.g. basic materials, number of layers, thickness).

e. The range of surface mounted components and associated materials shall be documented in the verification programme, including

1. For passive components: nature, types, sizes, termination finishes.
2. For active components: type of package, sizes, number of I/0, pitch, termination finishes.
3. Solder alloy composition, adhesives, conformal coating and printed circuit boards.

f. The verification test boards shall support at least three devices of each type and size of component which are assembled according to the PID specified in clause 5.

g. The supplier's repair process including removing and replacing of one of each type of mounted device shall be submitted to verification testing.

h. The configuration shall be submitted to a verification test programme as specified in subclause 14.3.

i. Any mounted package that has been verified on one class of substrate shall be considered verified on another substrate material that belongs to the same class as shown in Table 2 and has the same surface finish.

j. Verification by similarity shall not be used for moisture sensitive components.

k. Verification testing of plastic encapsulated components shall be performed for each batch according to this clause.

l. A repair, not included in ECSS-Q-70-28A, shall be submitted to a verificiation test programme.

14.2 Verification by similarity

a. The assembly of intermediate sizes of SMD, of a same package type, shall be considered approved when the smallest and largest devices pass the environmental test programmes made in accordance with this Standard.

NOTE SMD size is defined by the greatest distance between soldering points, which is the diagonal dimension, usually between corner leads. A square package is considered the same family as a rectangular package.

b. When the weight of the intermediate size of the device is not between the weight of the smallest and biggest device the verification by similarity shall not apply.

c. Packages belonging to the same family shall be constructed from the same materials.

d. The lead pitch and materials composition shall be identical.

e. The coated layers on the termination shall be identical.

f. The metallization of the termination and the barrier layers on leadless devices shall be identical.

g. Different lead forms (e.g. gullwing, J-leads, and LCC) shall be considered as different families.

h. Side-brazed, top-brazed and bottom-brazed packages shall be considered as different families.

i. Dual and quad-side pin arrangements shall be considered as different families.

j. Within a family the bending dimensions and shape shall be identical.

k. Verification by similarity shall not apply to plastic components.

14.3 Verification test programme

a. The verification test programme as shown in Figure 12 shall consist of:

1. Visual inspection according to clause 13.
2. Vibration testing according to subclause 14.5.

NOTE Mechanical testing according to this standard gives an indication of the reliability of the product in actual applications. It is unlikely that the test vehicle represents every flight configuration (size of the board, damping of the board, stiffening of board, number of board layers). The deflections, amplitudes, transmissibilities, radii of curvature experienced by SMDs under shock and vibration are totally dependant on the board to which they are mounted. Because each space project has its own unique shock and vibration requirements it is impossible to determine appropriate test levels without testing actual electronic boxes.

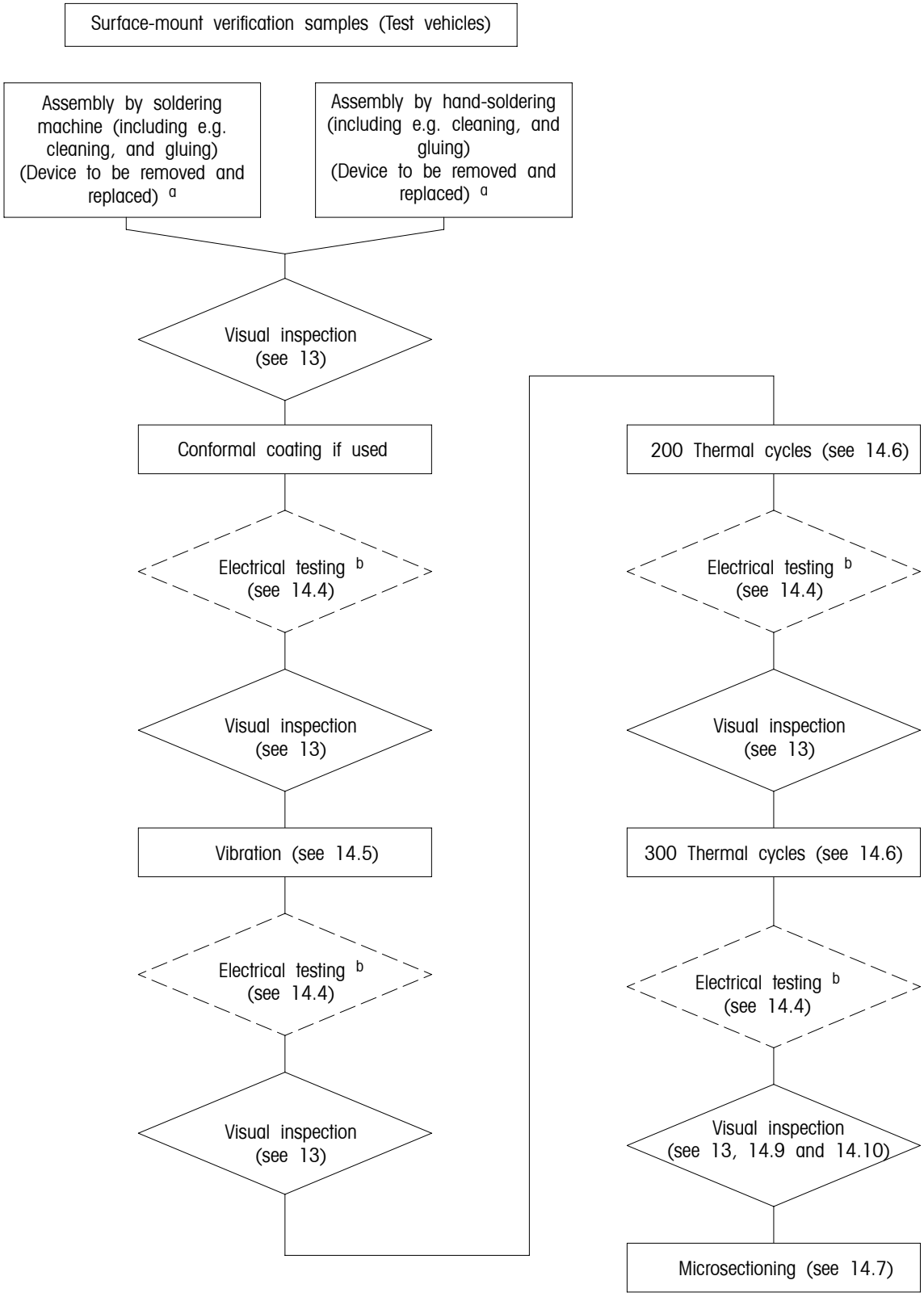
3. Temperature cycling according to subclause 14.6 except for area array devices where temperature cycling is according to subclause 14.9.2.

NOTE Temperature cycling is performed to ensure that the SMDs, substrates, solder alloys and associated staking compounds and conformal coatings are suitable for the operational lifetime of the spacecraft.

4. Microsectioning and dye-penetrant testing according to subclauses 14.7 and 14.8.

b. The supplier shall present a verification programme for approval.

NOTE Owing to the different modes of failure resulting from vibration and temperature cycling, the supplier can use any sequence of environmental testing.



[a] This validates the repair of each type of device removed and replaced.

[b] Electrical testing is recommended. It is good practice to perform the vibration and thermal cycling testing under electrical monitoring

Figure 12: Verification programme flow chart

14.4 Electrical testing of passive components

When passive components are functionally tested, and when continuity tests on series-connected packages are made using internal wiring of packages (daisy–chain):

a. No signal loss shall be accepted.

NOTE 1 When performed, electrical testing can best be conducted during the complete thermal cycle.

NOTE 2 Devices can be interconnected to multilayered circuit boards.

b. A drift of less than 10 % of resistance shall be accepted when the continuity tests are performed at room temperature.

NOTE Devices having soldered connections that cannot be inspected (due to access, small size or opaque conformal coating) are expected to be monitored during environmental testing by electrical test.

14.5 Vibration

ECSS-Q-70-08A, subclause 13.3 shall apply.

14.6 Temperature cycling test

a. ECSS-Q-70-08A, subclause 13.2 shall apply for the thermal profile.

b. The total number of temperature cycles shall be 500, except for area array devices with conformal coating when subclause 14.9.2. is applicable.

c. The monitoring thermocouple shall be attached to the surface of the printed circuit board.

d. Temperature cycling may be performed before the vibration testing. Vibration testing may be performed after any number of temperature cycles.

14.7 Microsection

a. At least one microsection shall be made after environmental testing on each type of device, size and process (machine assembly and manual soldering).

NOTE Examples of microsections are shown in subclause 16.4.

b. The microsection shall be done on the device having the worst solder joint appearance.

NOTE Generally this is on the interconnections closest to the corners of the device.

c. The microsection shall be made even if all similar devices have no indication of surface cracks

NOTE The reason is that there can be cracks in the interconnection.

d. The Approval authority shall have access to the microsection.

e. The microsections shall be stored for a period of at least 10 years.

NOTE Stored samples can assist the analysis of in-service failures.

14.8 Dye penetrant test

a. At least one BGA or CGA shall be submitted to a dye penetrant test.

NOTE A typical dye penetrant test is described in C.4.5.

b. The dye penetrant test results and samples shall be stored for a period of at least 10 years.

NOTE Stored samples can assist the analysis of in-service failures.

14.9 Special verification testing for conformally coated area array packages

14.9.1 Introduction

BGA and CGA packages are generally assembled and then conformally coated. When the conformal coating cannot be removed it prevents the use of dye penetrant testing.

When the device is conformally coated, as no other test can evaluate all the I/O connections after environmental testing, a special programme is developed.

NOTE Conformal coatings and underfills can lead to non-inspectability and difficulties for rework or repair.

14.9.2 Provisions

a. When a device is conformally coated, the supplier shall submit a special programme for approval.

b. The special programme specified in 14.9.2 a. shall consist of vibration testing in accordance with subclause 14.5 and at least 1 500 thermal cycles in accordance with subclause 14.6.

c. For devices other than MCGA, a data acquisition system, applying 5 V with monitoring current limited to 1 mA shall continuously monitor the electrical continuity of all I/O and for at least 10 cycles every 100 thermal cycles and the results recorded.

d. The system shall be capable of detecting open circuit durations exceeding 200 ms.

14.10 Failures after verification testing

a. Any electrical failures during or after testing shall invalidate the SMD verification.

b. In the case of visual failures, an analysis shall be performed to identify the cause: component or soldering process.

c. In the case of cracked joints, microsections shall be made to evaluate their depth and origin.

d. Surface and internal cracks that penetrate less than 25 % of the solder fillet critical zone (as defined in Figure 13), ball or column, shall be considered acceptable.

e. Cracks present outside the critical zone shall be considered acceptable.

f. Cracks in the intermetallic layer in solder joints to area array devices shall be considered as not acceptable.

g. After removing the area array device during the dye penetrant test the dye penetrant shall not cover more than 25 % of the ruptured solder joint area.

NOTE 1 See C.4.5 for an example of dye penetrant test.

NOTE 2 See also clause 16 Figures 54 to 56 for details.

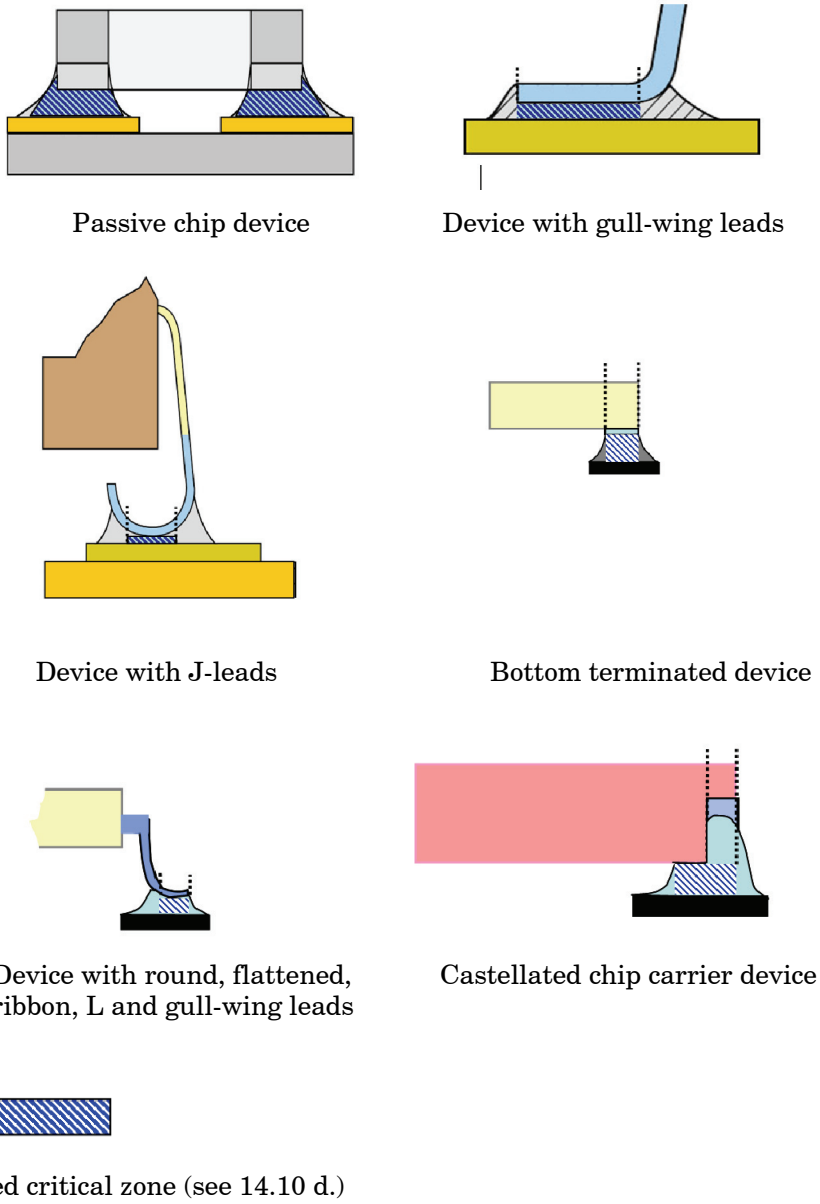


Figure 13: Illustrations defining critical zone in solder fillet

14.11 Approval of verification

a. A letter confirming the completion of a successful verification programme shall be sent to the contact person of the supplier, with the summary table specified in Annex B attached to it.

NOTE 1 The letter and the summary table provide evidence of the verification approval to a third party.

NOTE 2 The approval of verification applies to all space projects from the date of the approval until withdrawn.

b. Every two years the supplier shall submit an updating of the SMT approval status.

c. When the materials used, or component types or processing parameters change, the supplier shall submit for approval to the Approval authority, a delta-verification programme.

d. Reference to the summary table number shall be made on each space project declared processes list in order to assist in achieving project approval.

NOTE See ECSS-Q-70B, Table D-3.

14.12 Withdrawal of approval status

The approval status of the supplier shall be withdrawn when any of the following status justify its withdrawal:

a. Repetetive supply problems and manufacturing defects.

b. Undeclared changes to the PID.

c. Continuous non-compliance with the PID.

15

Quality assurance

15.1 General

ECSS-Q-20B shall apply.

15.2 Data

ECSS-Q-70-08A, subclause 14.2 shall apply.

15.3 Nonconformance

ECSS-Q-20-09B shall apply.

15.4 Calibration

ECSS-Q-70-08A, subclause 14.4 shall apply

15.5 Traceability

ECSS-Q-70-08A, subclause 14.5 shall apply.

15.6 Workmanship standards

a. ECSS-Q-70-08A, subclause 14.6 shall apply.

b. Visual standards consisting of work samples or visual aids that illustrate the quality characteristics of all soldered connections involved shall be prepared and be available to each operator and inspector.

NOTE The illustrations presented in clause 16 of this Standard can be included as part of the examples.

15.7 Inspection

a. During all stages of the process, the inspection points defined in the manufacturing flow chart shall be carried out.

b. The inspection shall be performed according to clause 13 of this Standard.

c. The inspection shall also include the substrate, components and component position in accordance with subclauses 11.5.1 to 11.5.8.

15.8 Operator and inspector training and certification

a. ECSS-Q-70-08A, subclause 14.8 shall apply.

b. A training programme for operators performing machine soldering shall be developed, maintained and implemented by the supplier to provide excellence of workmanship and personal skill in SMTs.

NOTE Records of training, testing and certification status of the soldering operators are maintained for at least 10 years.

c. Operators performing hand soldering of SMDs, and inspectors of SMD and mixed-technology assemblies shall be trained and certified at a school authorised by the final customer.

15.9 Quality records

The quality records shall be made of, as a minimum, the following:

a. PID (including the summary tables and workmanship standards).

b. Audit report established by the approval authority.

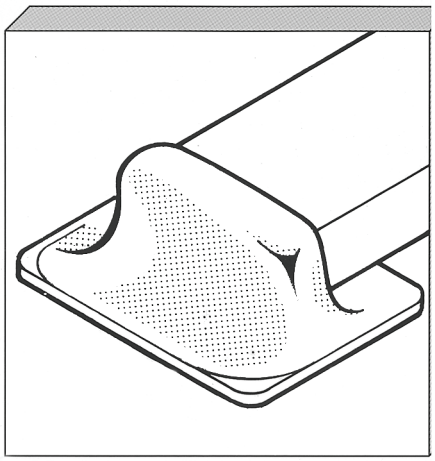
c. Verification report, as output of the verification test programme.

16

Visual and X-ray workmanship standards

16.1 Workmanship illustrations for standard SMDs

16.1.1 Chip components



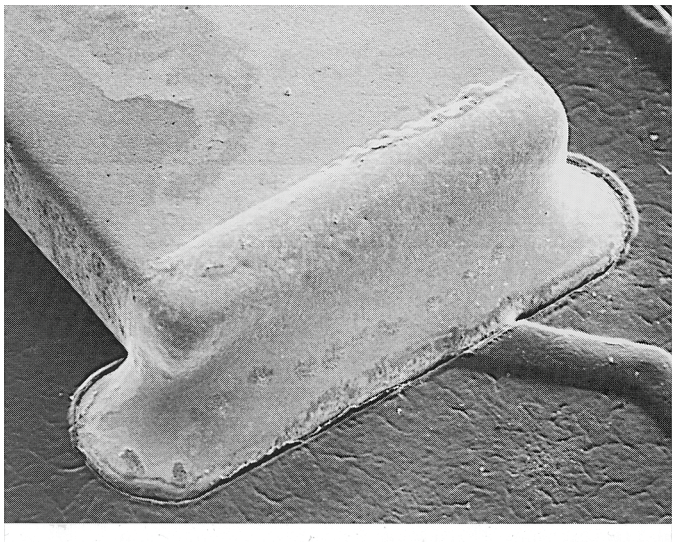
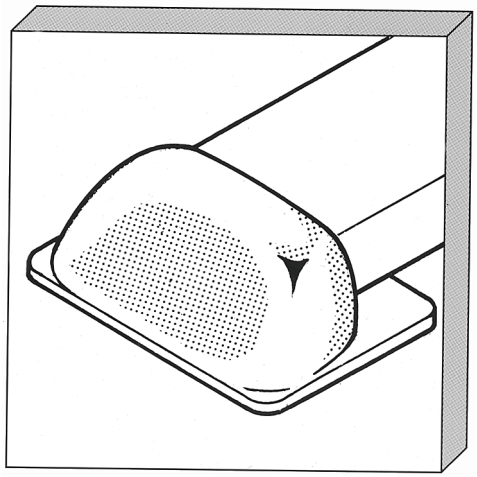


Figure 14: Preferred solder (see also Table 3)



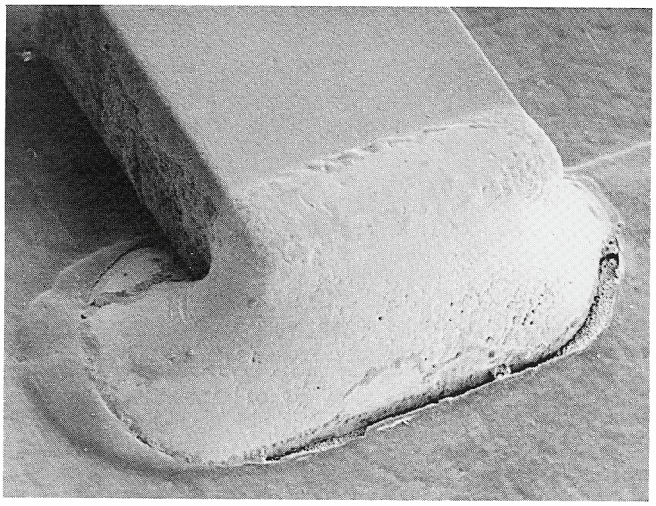
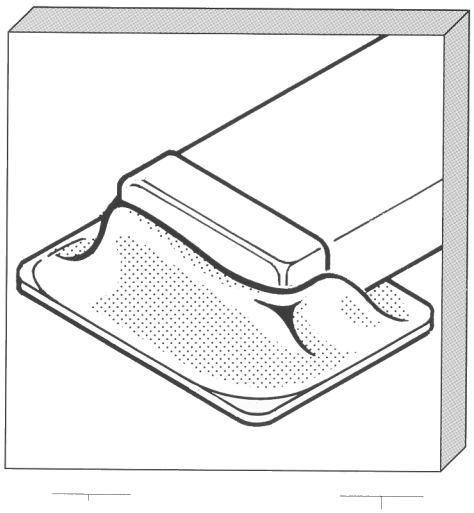


Figure 15: Acceptable, maximum solder (see also Table 3)



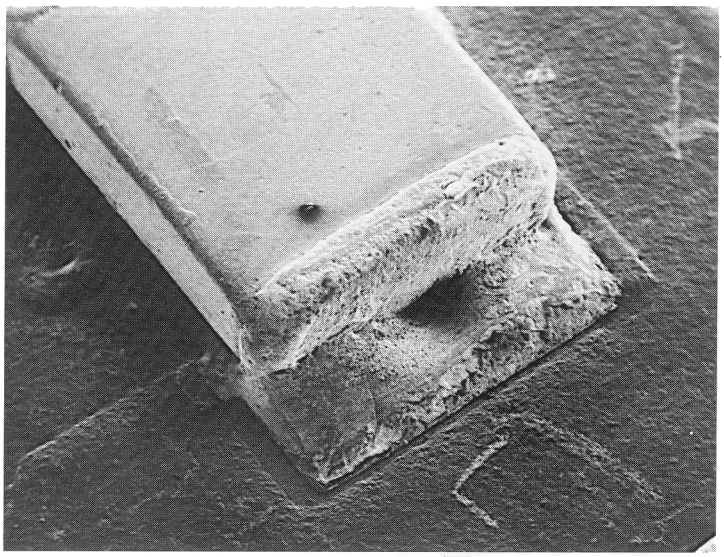
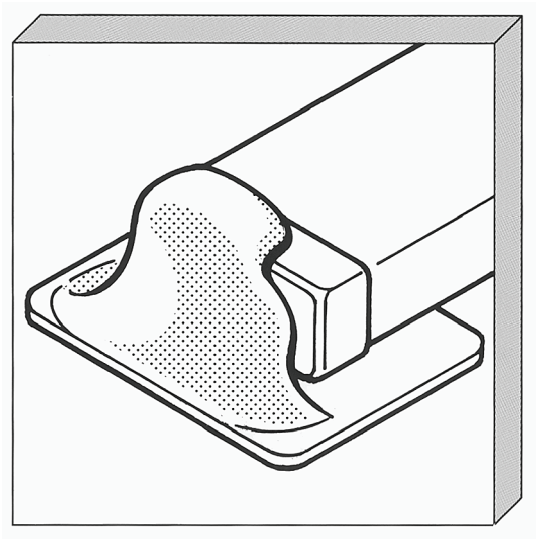


Figure 16: Unacceptable, poor wetting (see also Table 3)



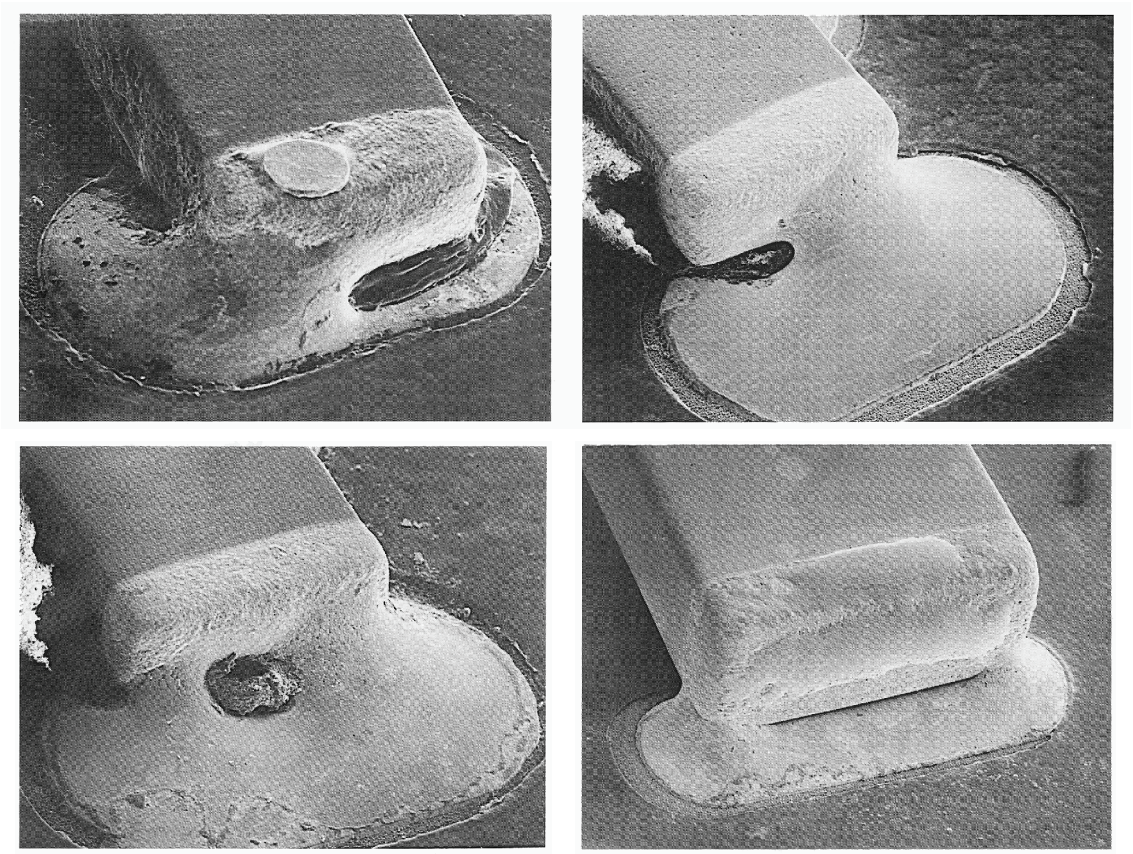


Figure 17: Unacceptable - Less than 75 % wetting of terminal edges
(see also Table 3)

16.1.2 MELF components

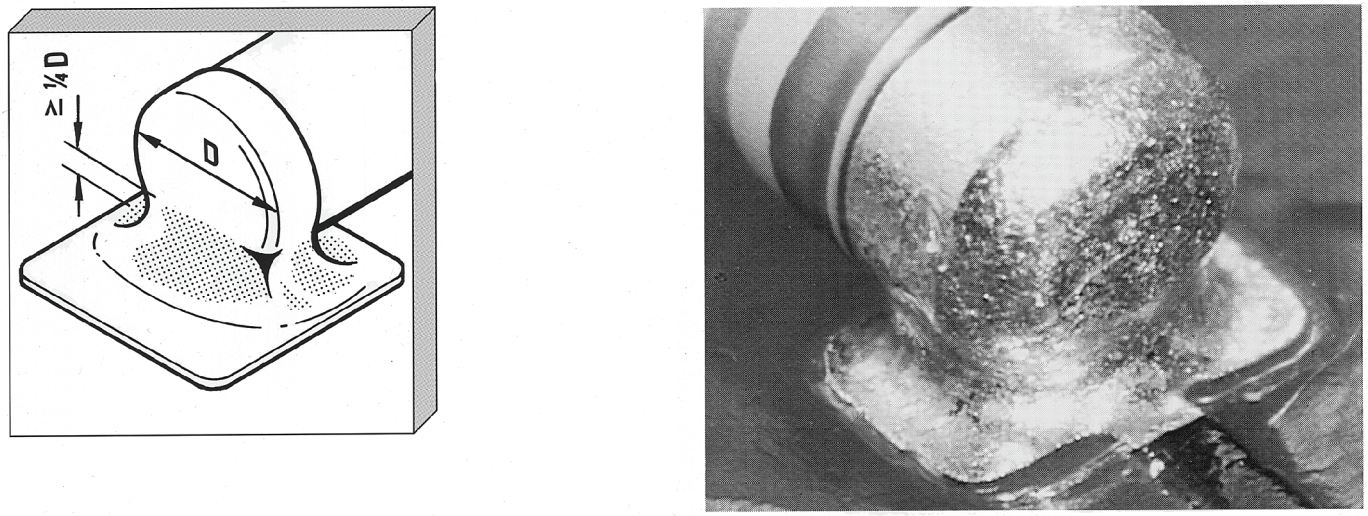


Figure 18: Acceptable, minimum solder - Terminal wetted along end, face and sides (see also Table 5)

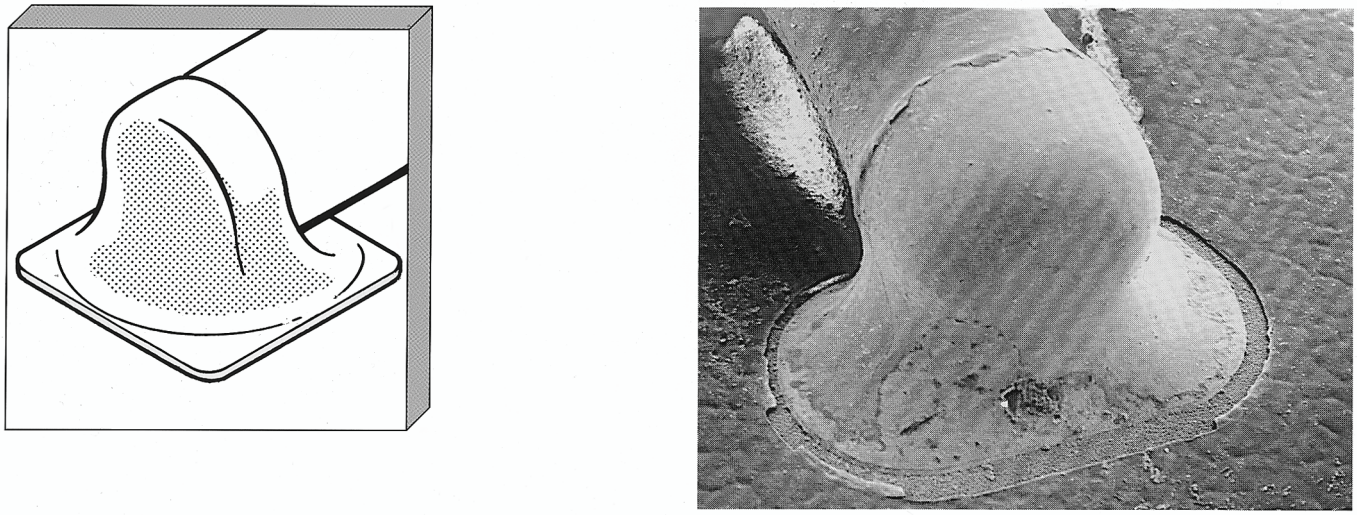
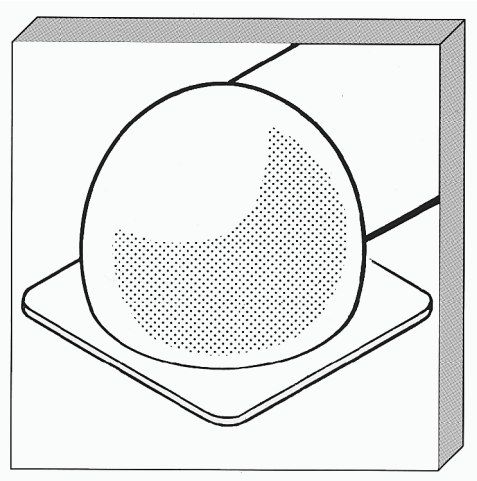


Figure 19: Preferred solder (see also Table 5)



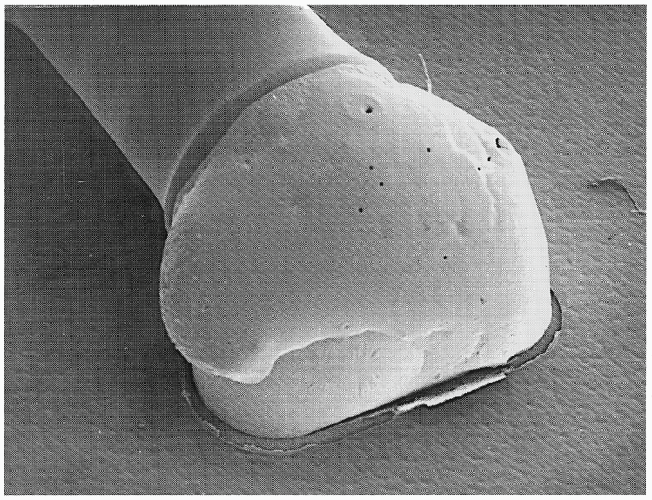
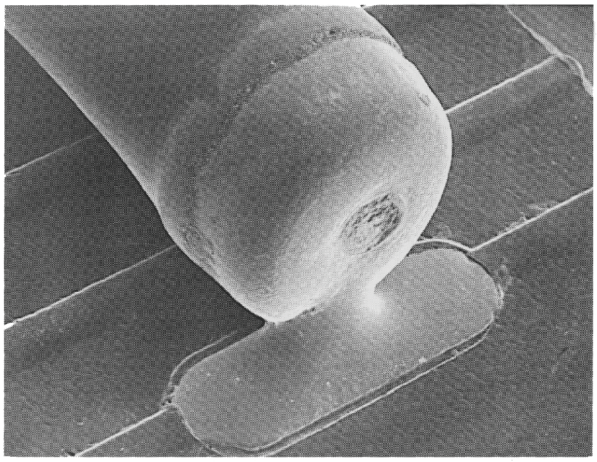


Figure 20: Unacceptable - Excessive solder (see also Table 5)



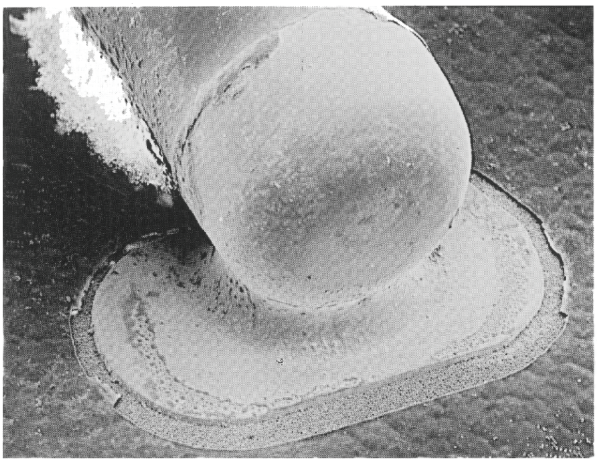
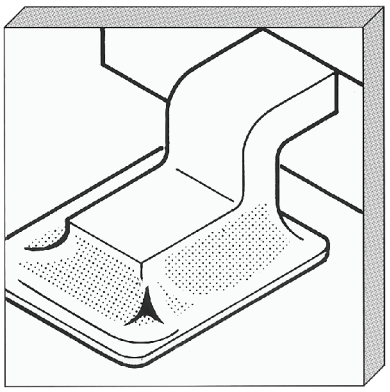
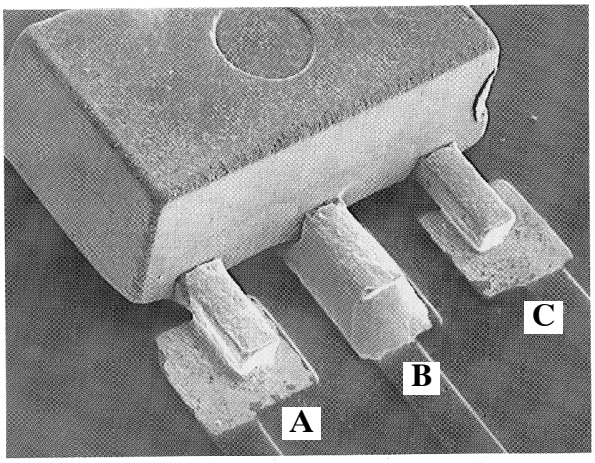


Figure 21: Unacceptable - Insufficient solder (see also Table 5)

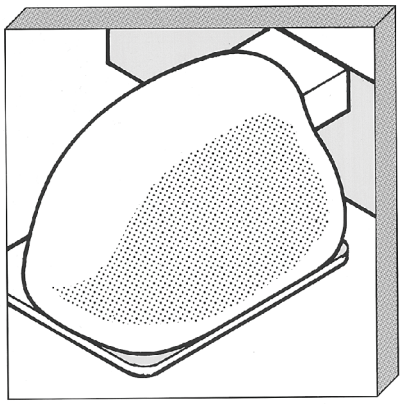
16.1.3 Ribbon, "L" and Gull-wing leaded devices





A = Acceptable minimum solder
B = Acceptable maximum solder
C = Insufficient solder

Figure 22: Example of flattened leads



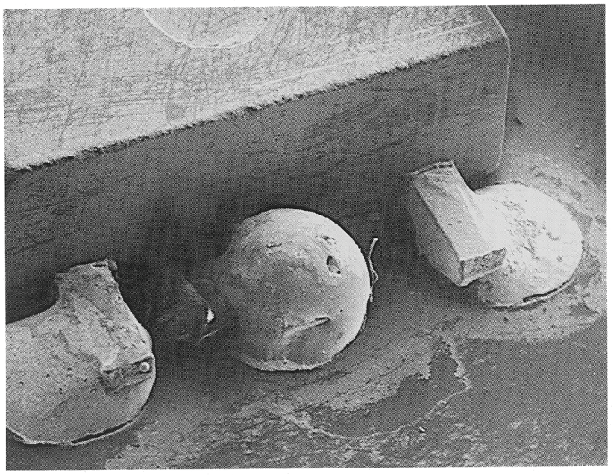
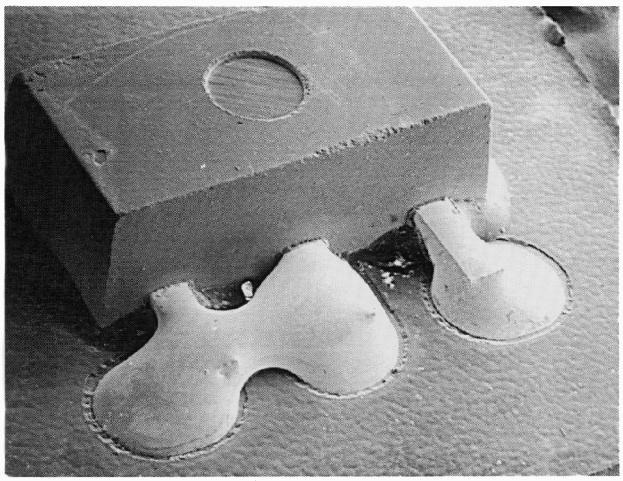
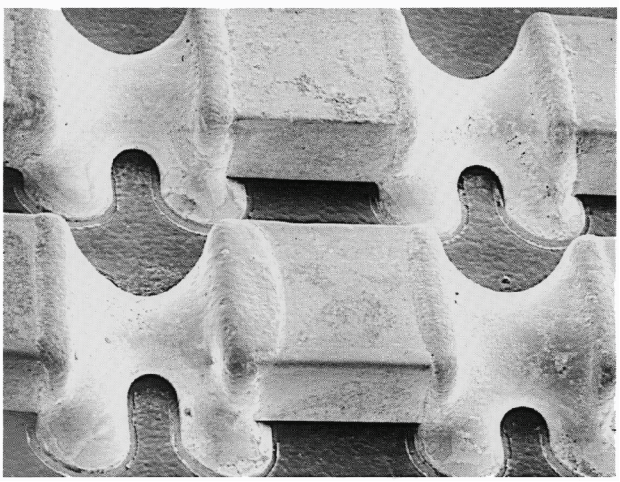


Figure 23: Unacceptable - Excessive solder (middle joint)

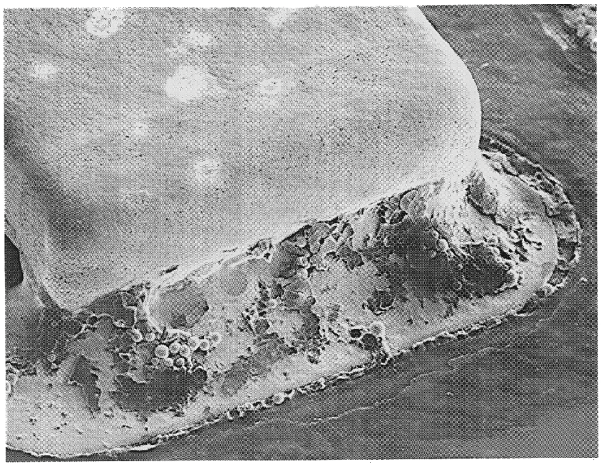
16.1.4 Miscellaneous soldering defects



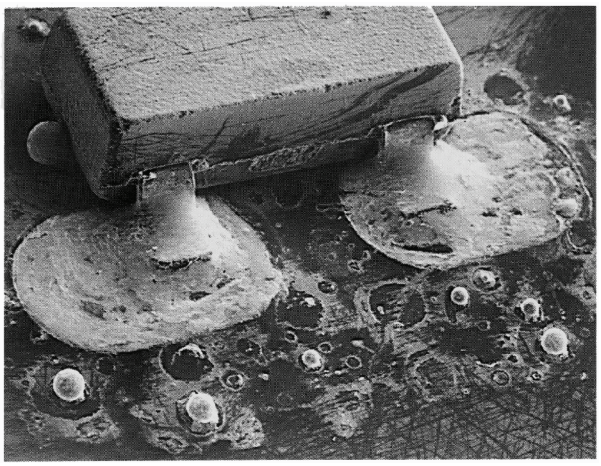
Unacceptable – Solder bridge between terminals



Unacceptable – Solder bridges between terminals



Unacceptable – Contaminated joint



Unacceptable – Solder balls

Figure 24: Examples of unacceptable soldering

16.2 Workmanship illustrations for ball grid array devices

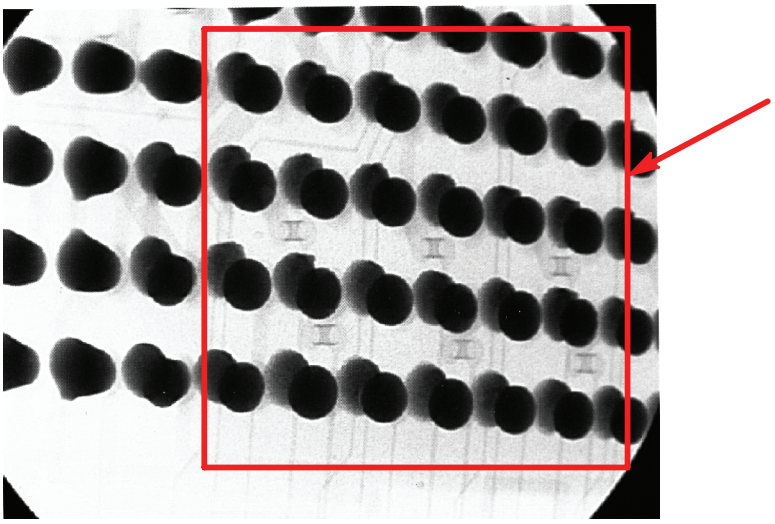
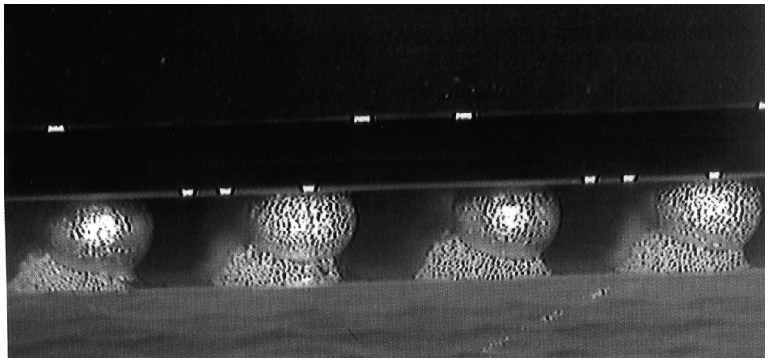


Figure 25: Angled-transmission X-radiograph showing solder paste shadow due to partial reflow: Reject



— non-reflow of solder paste: Reject.

— maximum misplacement (15% of pad ∅): Accept.

Figure 26: Micrograph showing

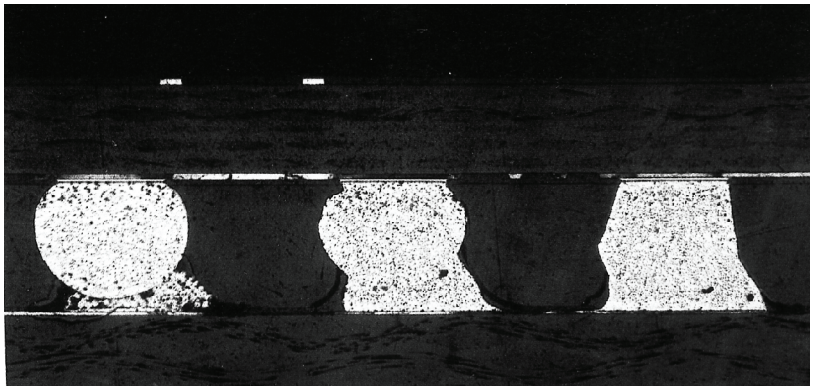
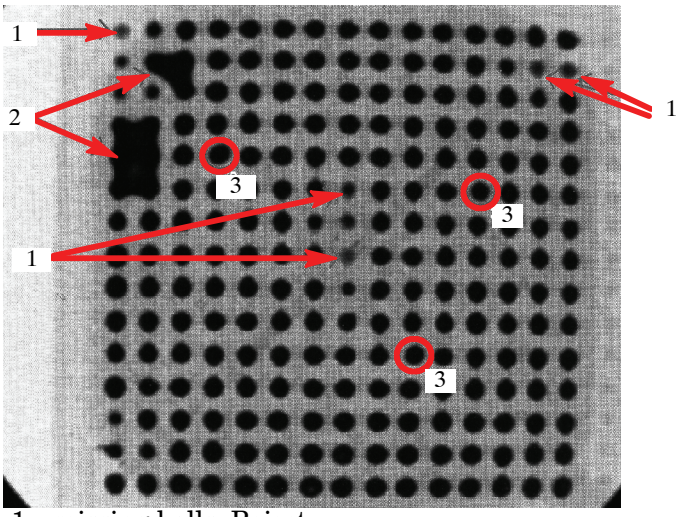
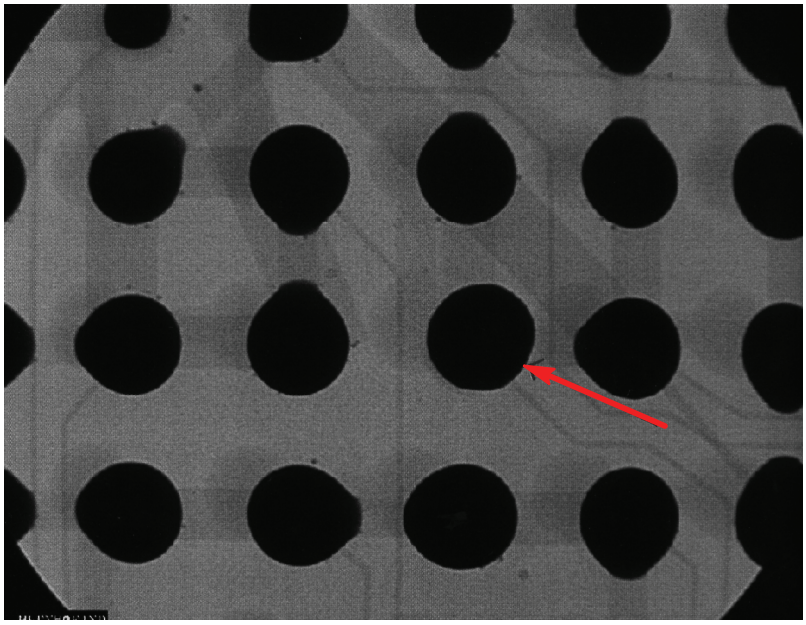


Figure 27: Microsection showing partial reflow of solder paste: Reject



1. missing balls: Reject
2. bridges: Reject
3. non-wetted pads: Reject

Figure 28: Perpendicular transmission X-radiograph showing unacceptable defects



Solder has not flowed to extent of teardrop pad: Reject

Figure 29: Perpendicular transmission X-radiograph showing non-wetted pad

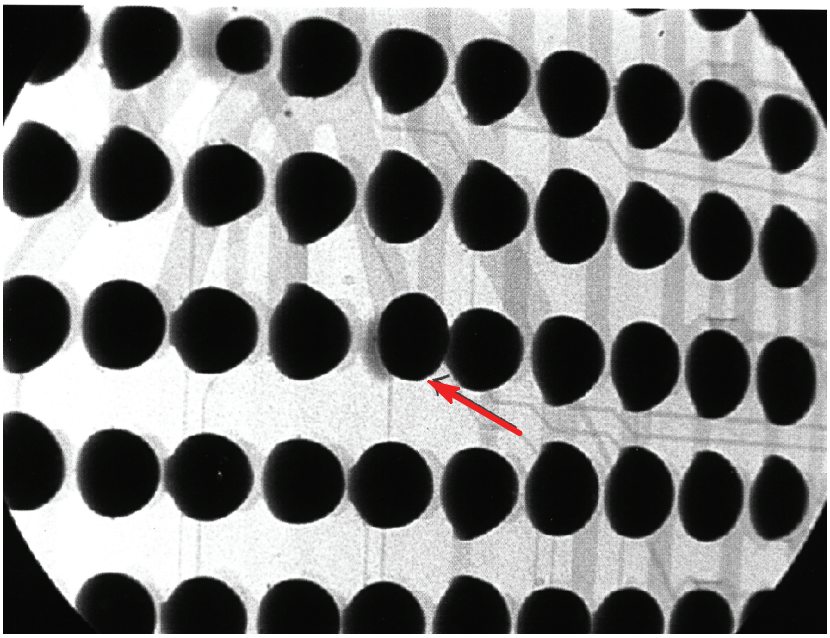


Figure 30: Angled transmission X-radiograph showing non-wetted pad: Reject

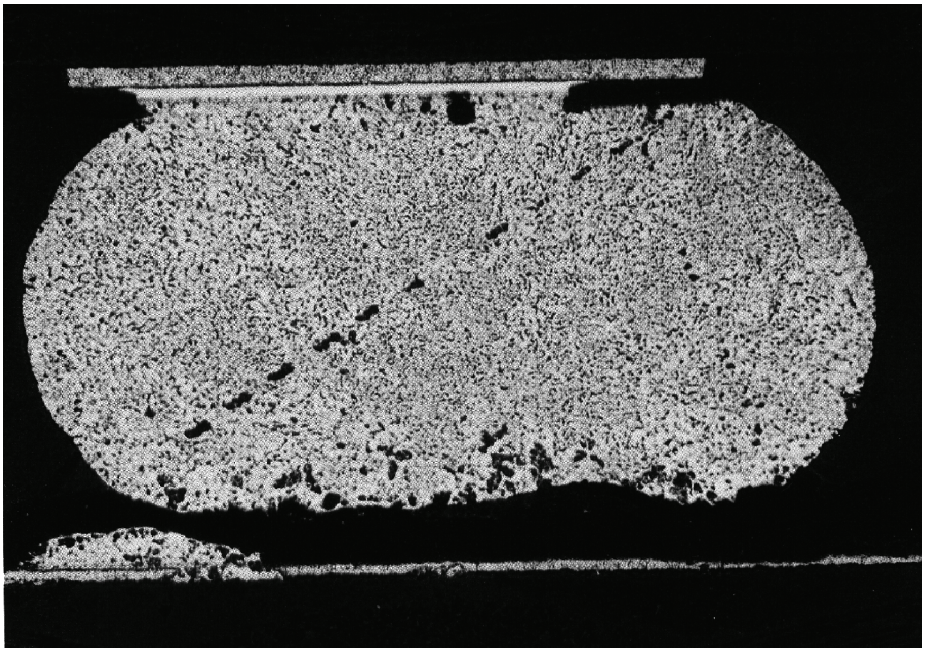


Figure 31: Microsection through a ball showing non-wetting of solder to pad: Reject

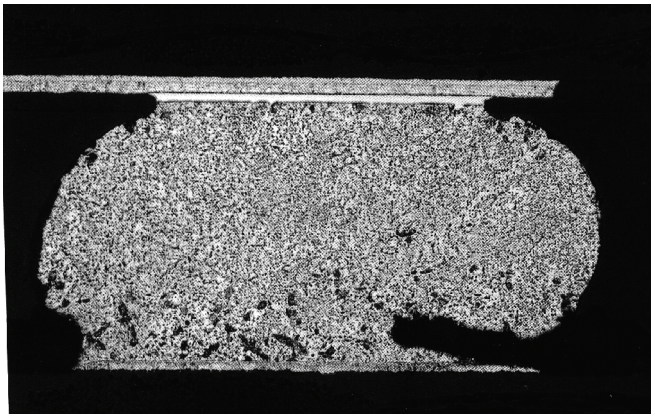


Figure 32: Microsection through ball showing partial wetting of solder to pad: Reject

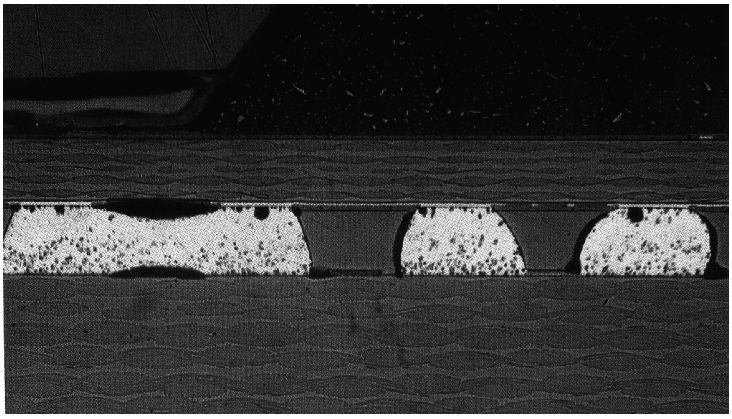
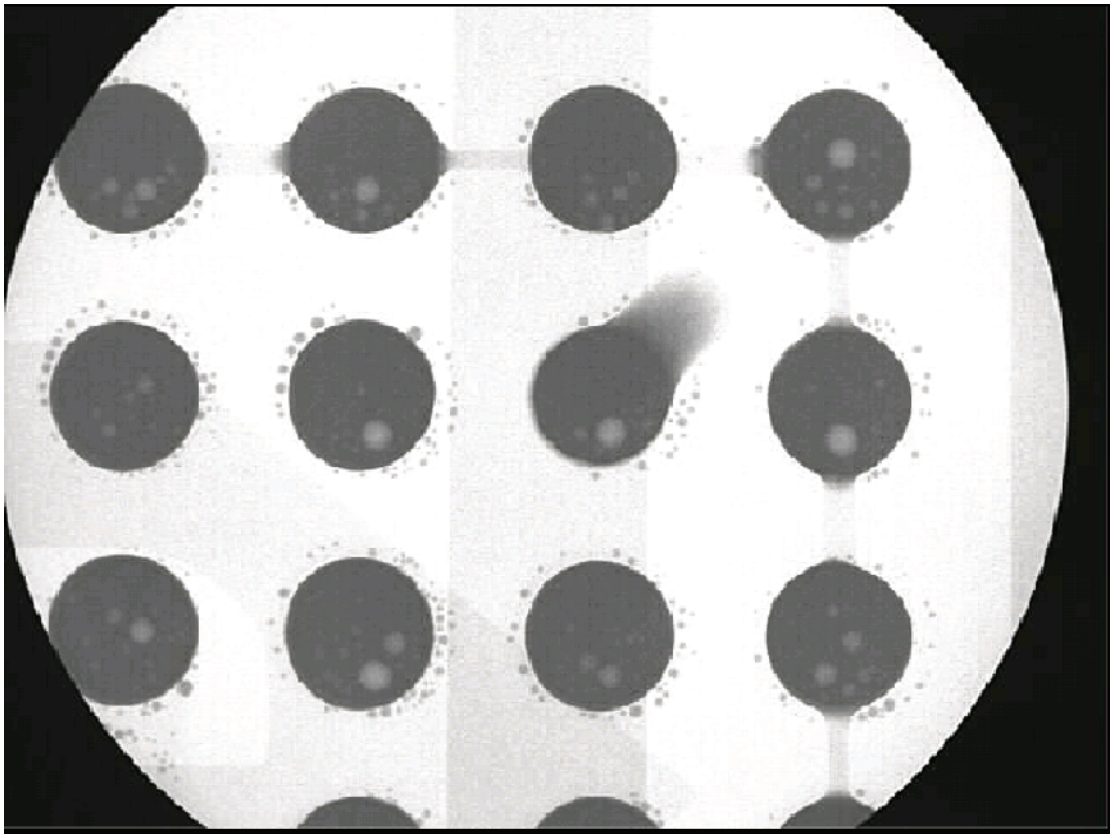


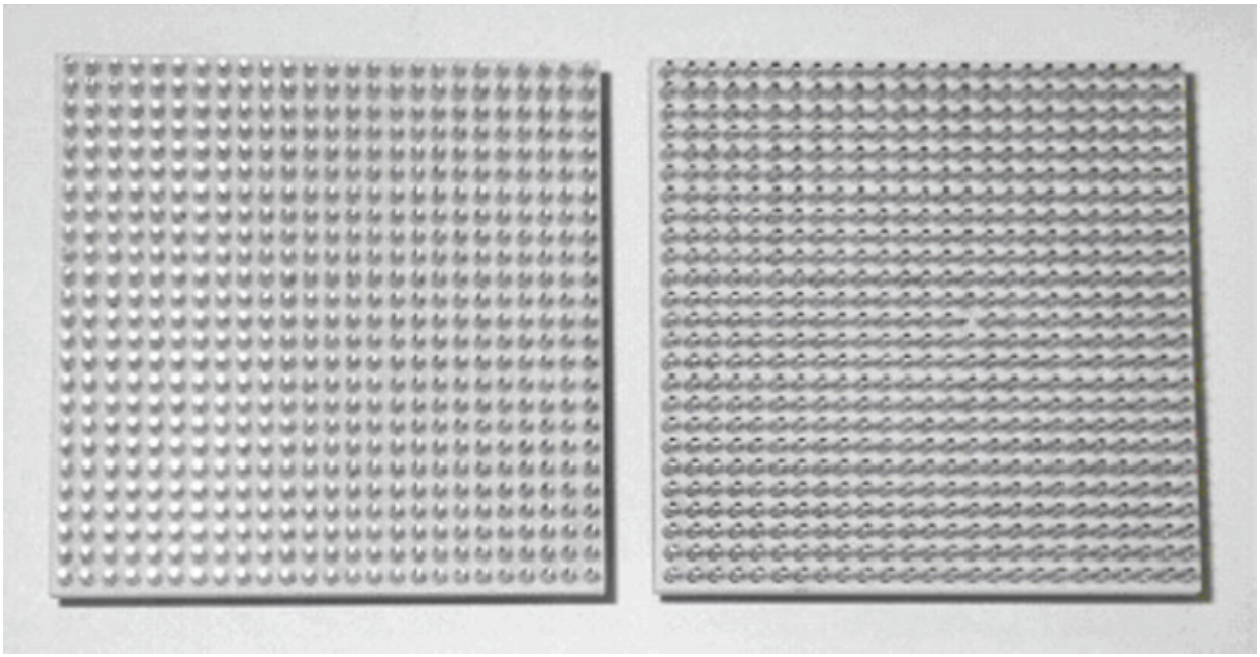
Figure 33: Microsection through ball showing solder bridge: Reject



Sum of voids in some BGA balls exceeds 25 % of ball's cross section diameter: Reject

Figure 34: X-radiograph showing many small voids and solder balls: Reject

16.3 Workmanship illustrations for column grid array devices



Good consistency of column alignment: Accept

Missing column: Reject.

Figure 35: Underside view showing

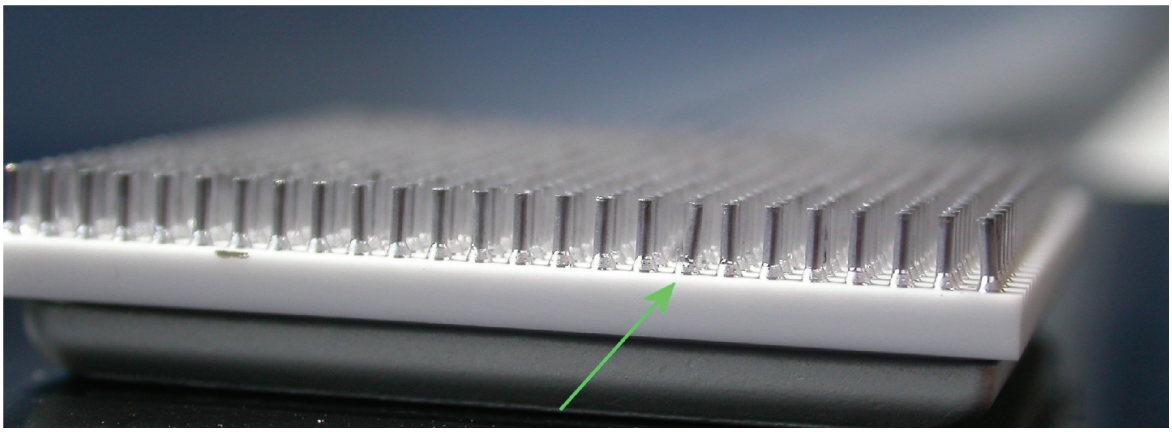


Figure 36: Side view showing column column by more than 5°: Reject

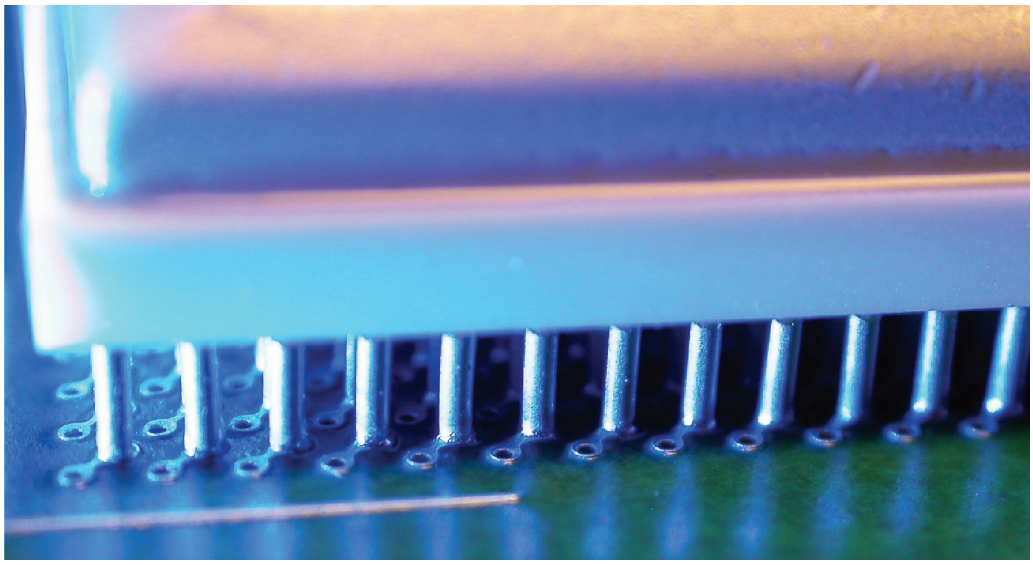
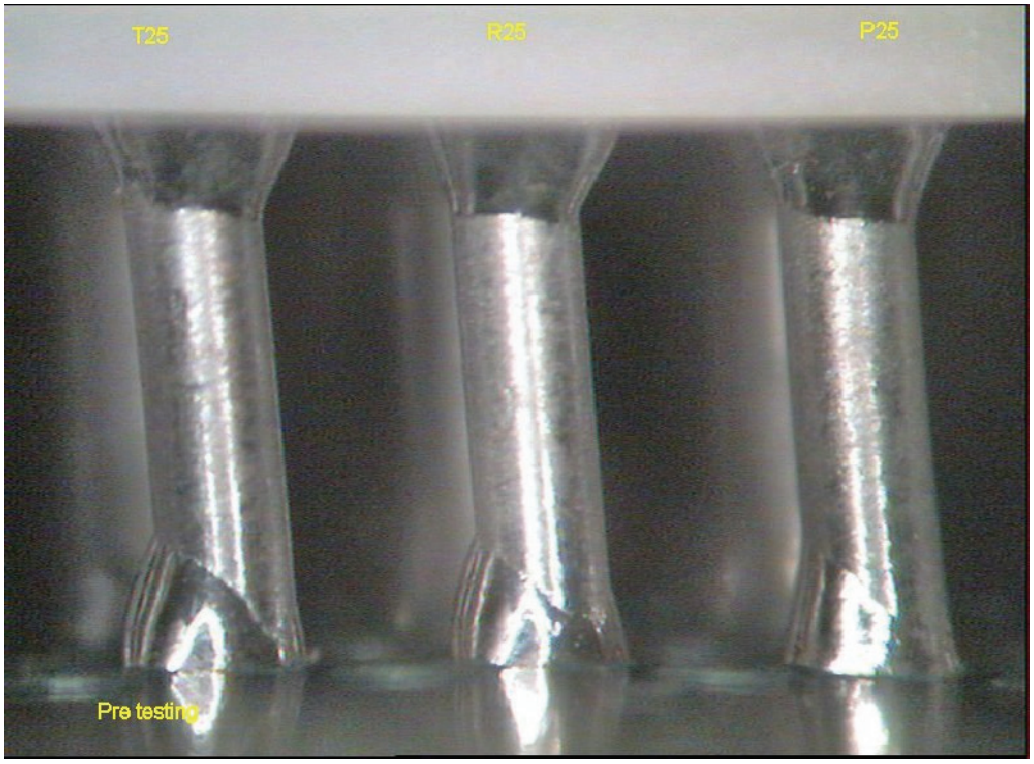
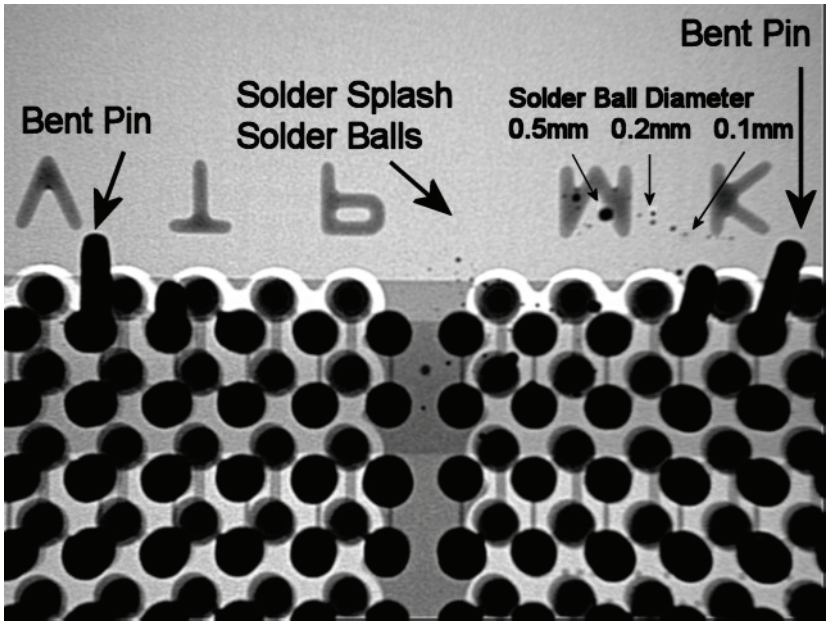


Figure 37: CGA mounted on PCB showing perpendicular columns centrally placed on pads: Target condition



Note: Asymmetry of solder fillets at PCB is consequence of teardrop pads and is acceptable

Figure 38: CGA mounted on PCB showing columns tilted < 5°: Accept



Bent columns (pins): Reject

Solder balls: Reject

Figure 39: X-radiograph of CGA mounted on PCB

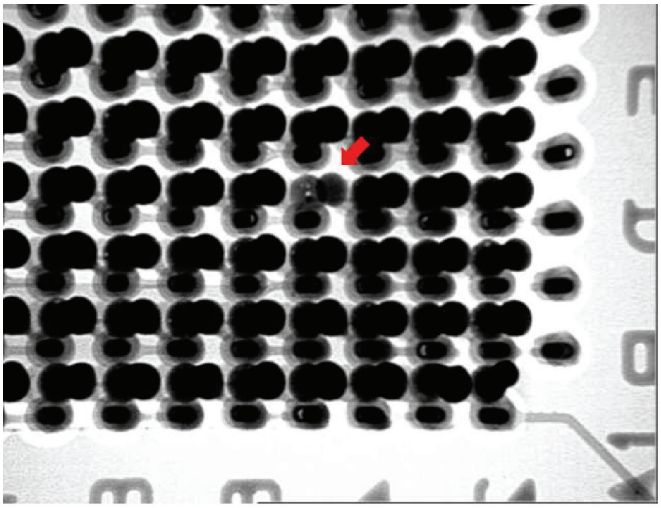


Figure 40: X-radiograph of CGA mounted on PCB showing missing column: Reject

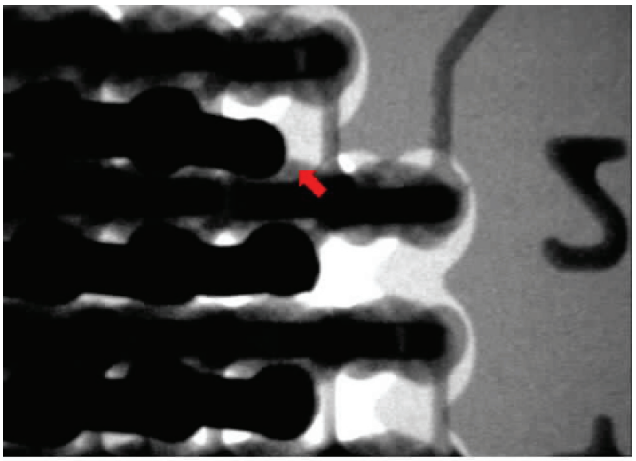


Figure 41: X-radiograph of CGA mounted on PCB showing insufficient solder: Reject

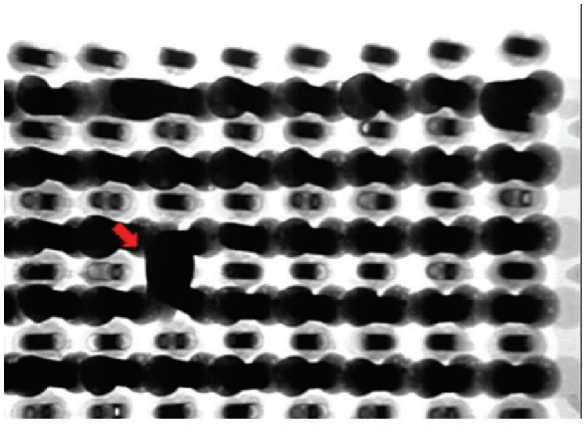


Figure 42: X-radiograph of CGA mounted on PCB showing solder bridge: Reject

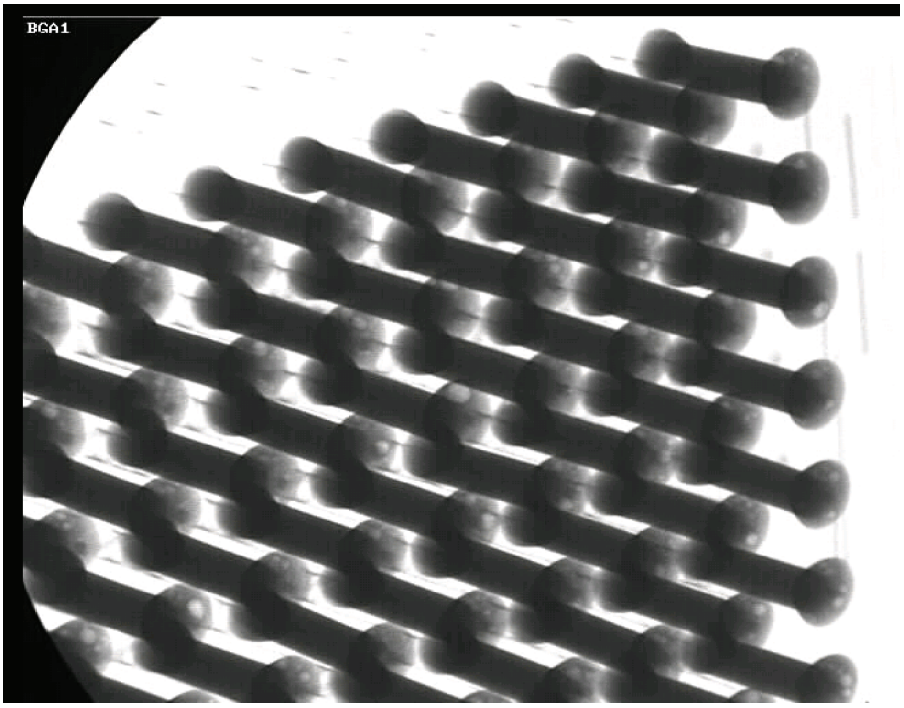
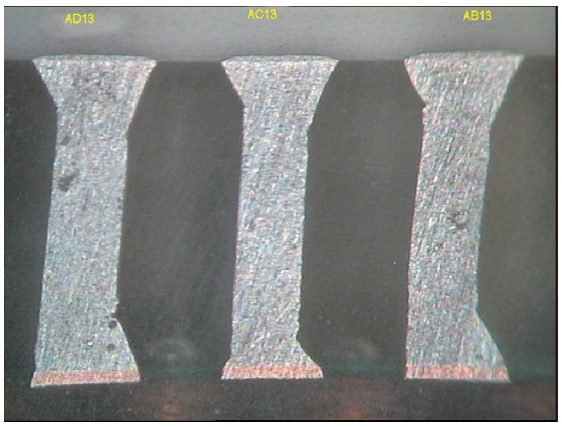


Figure 43: X-radiograph of CGA showing excessive voiding in solder fillets at base of columns: Reject

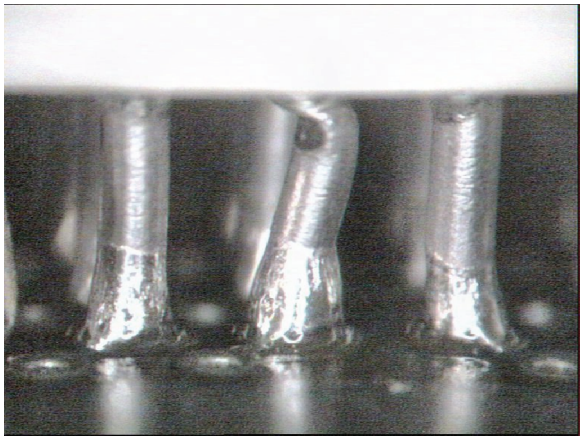


Good solder fillets at PCB: Accept

Note: Asymmetry of solder fillets at PCB is consequence of teardrop pads and is acceptable.

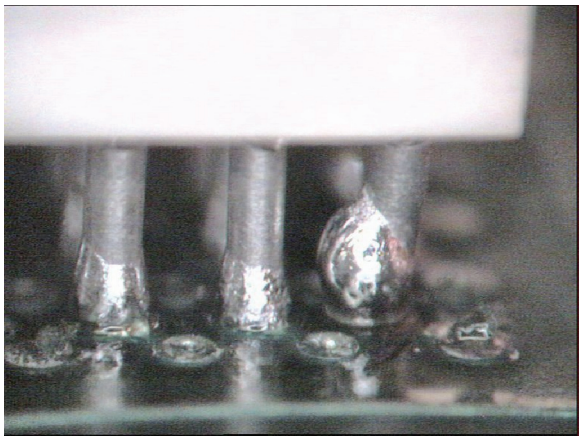
Solder fillets at package undisturbed by reflow process: Accept.

Figure 44: Microsection of CGA mounted on PCB



Bent column: Reject

Figure 45: Micrograph of CGA mounted on PCB



Unsoldered column: Reject.

Figure 46: Micrograph of CGA mounted on PCB

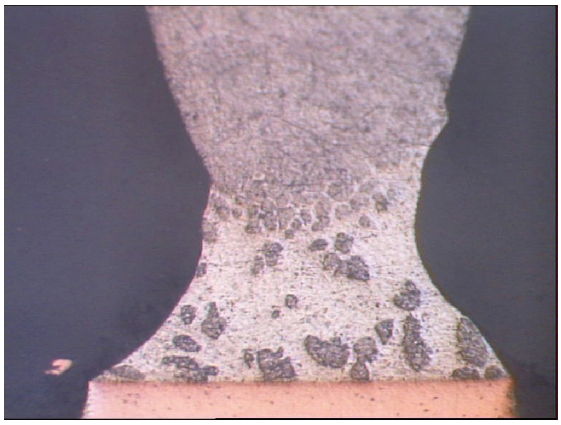


Figure 47: Microsection of CGA mounted on PCB showing minimum solder: Acceptable

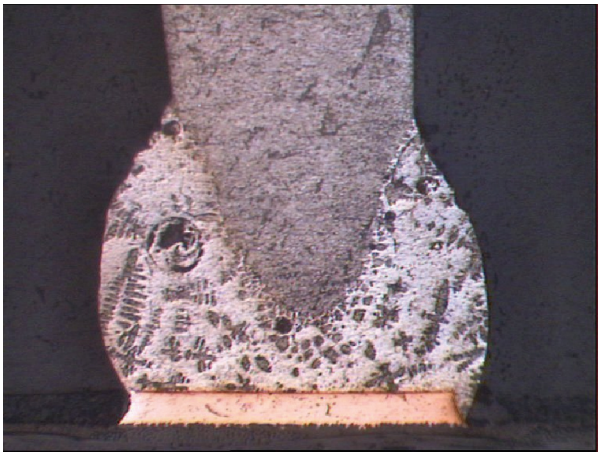
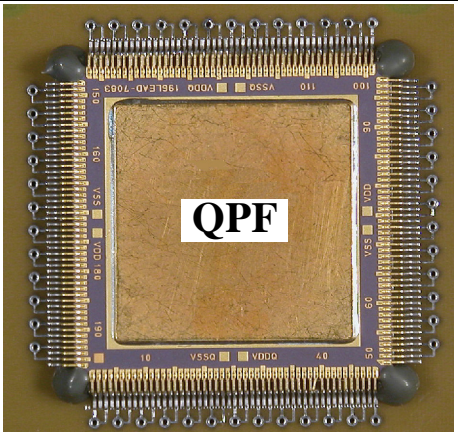
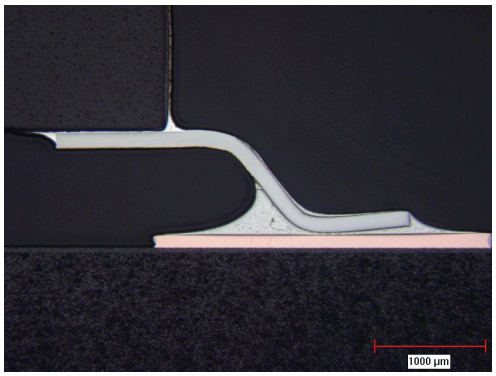
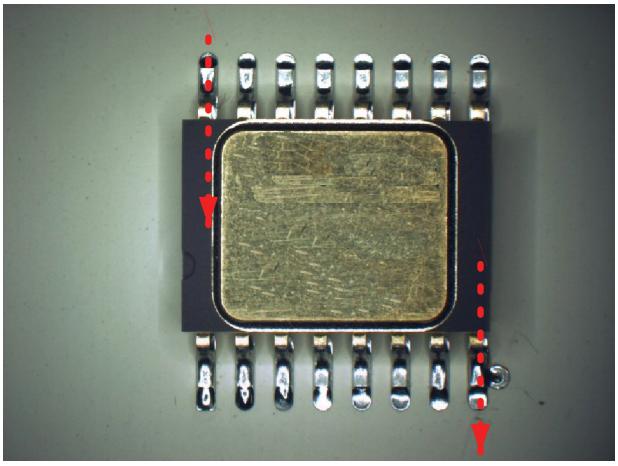
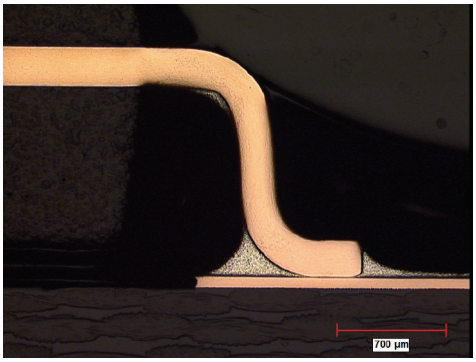
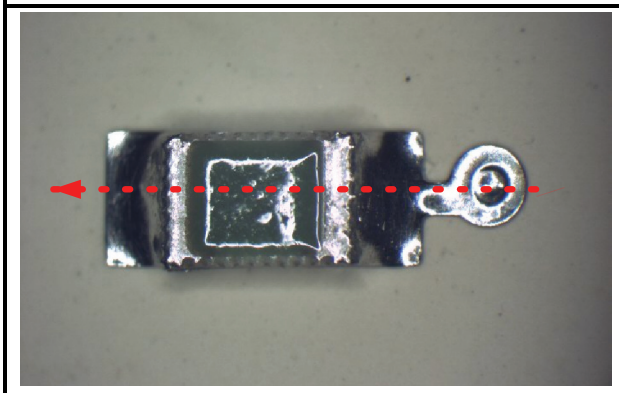
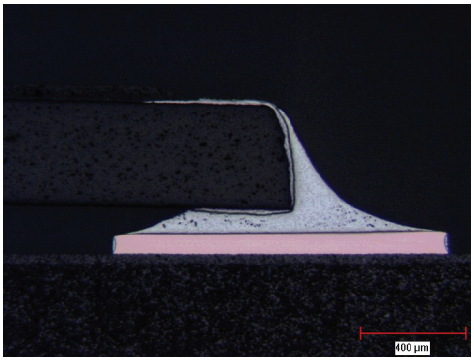
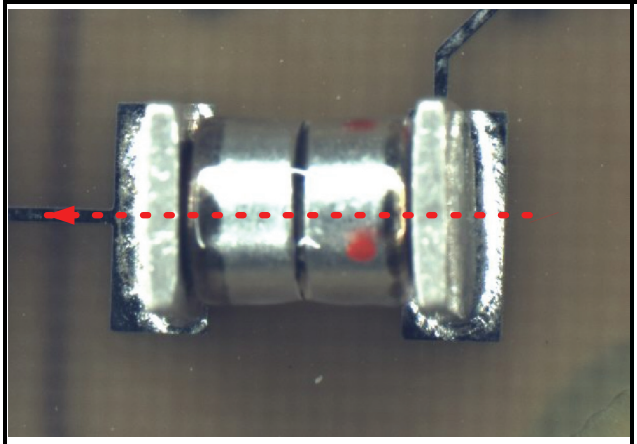
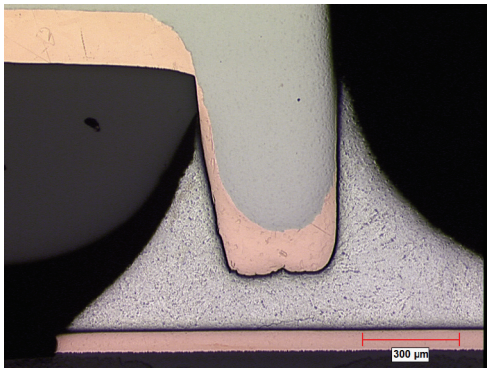
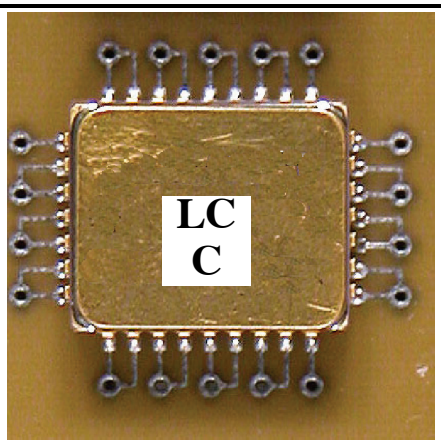
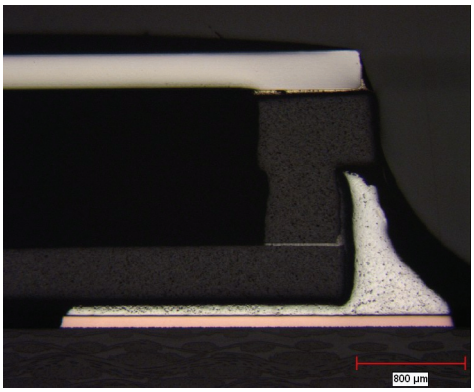
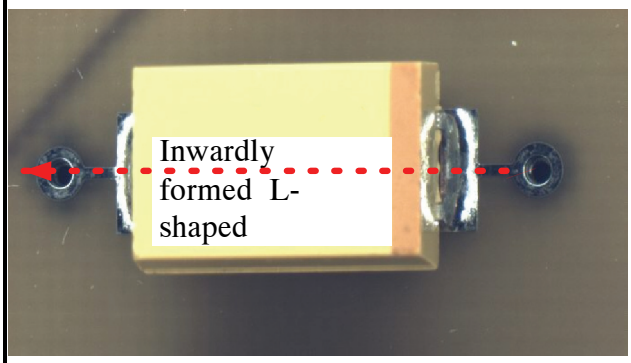
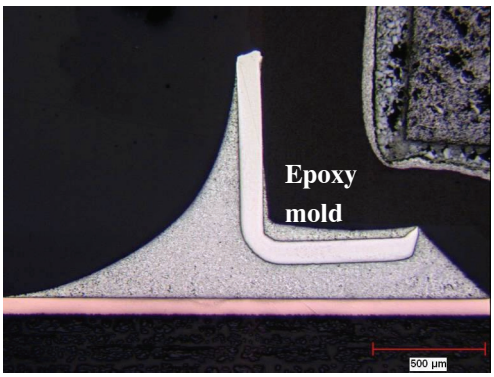
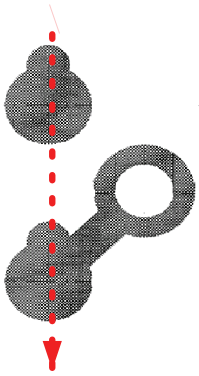
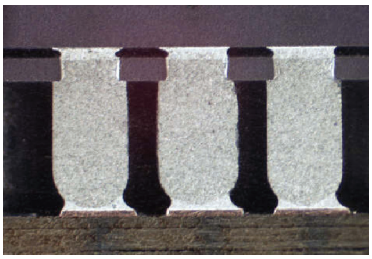
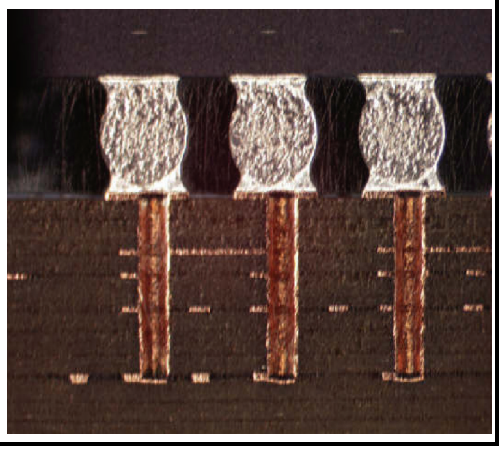


Figure 48: Microsection of CGA mounted on PCB showing maximum solder: Acceptable

16.4 Microsection examples

Device package	Microsection
	
	

Device package	Microsection
	
	
	

Device package	Microsection
	
	 

16.5 Accept and reject criteria after environmental testing

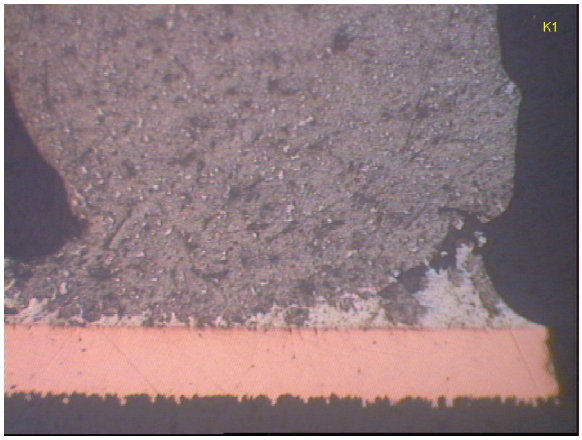
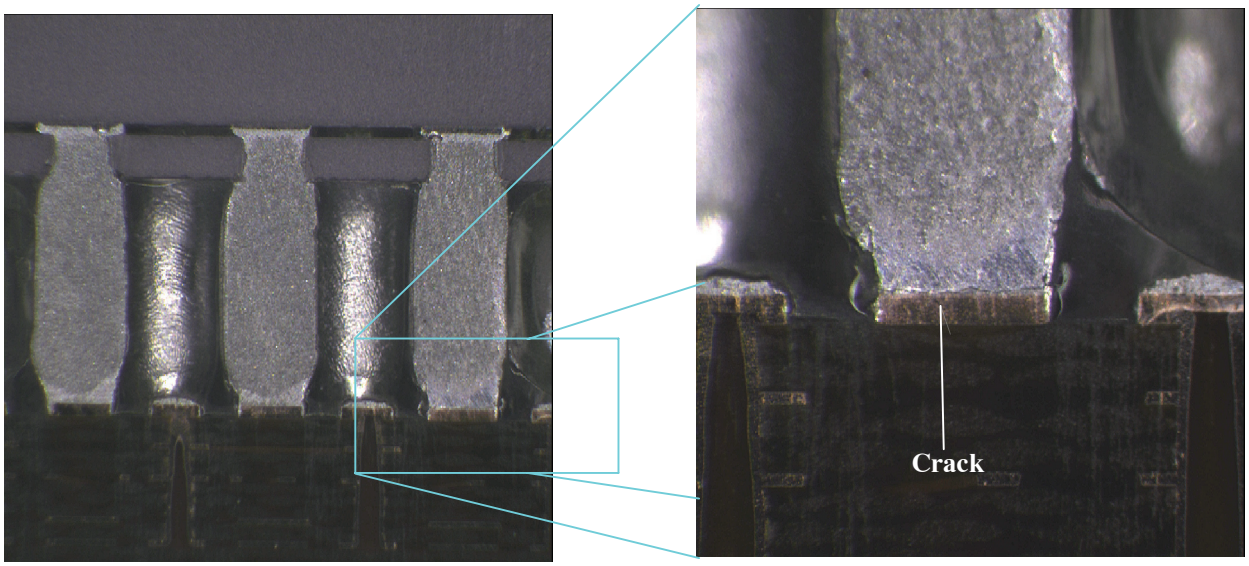
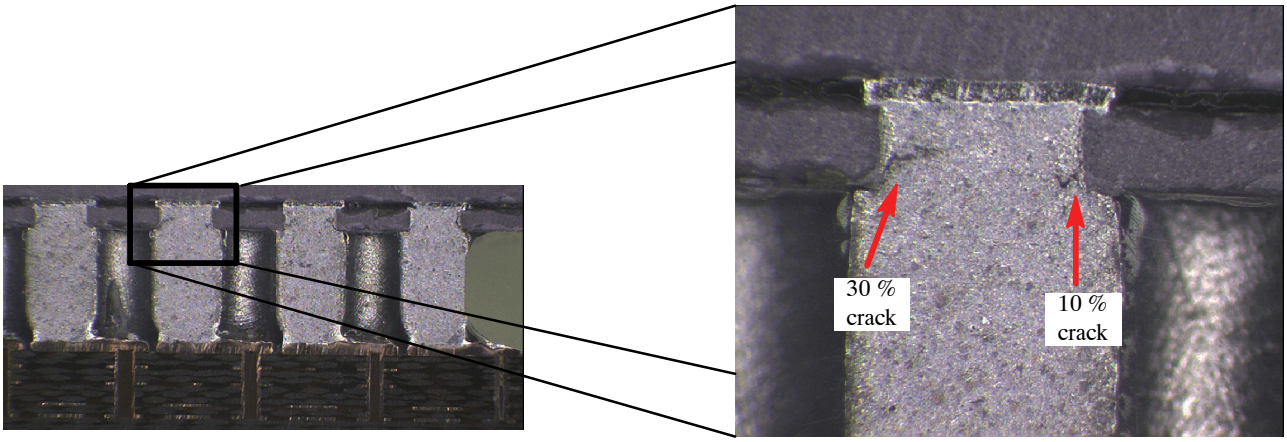


Figure 49: Sample after verification sample testing: Microsection of CGA mounted on PCB showing crack in the solder fillet



A fatal crack located in the solder joint between the column and the pad. The crack goes through the whole solder joint: Reject

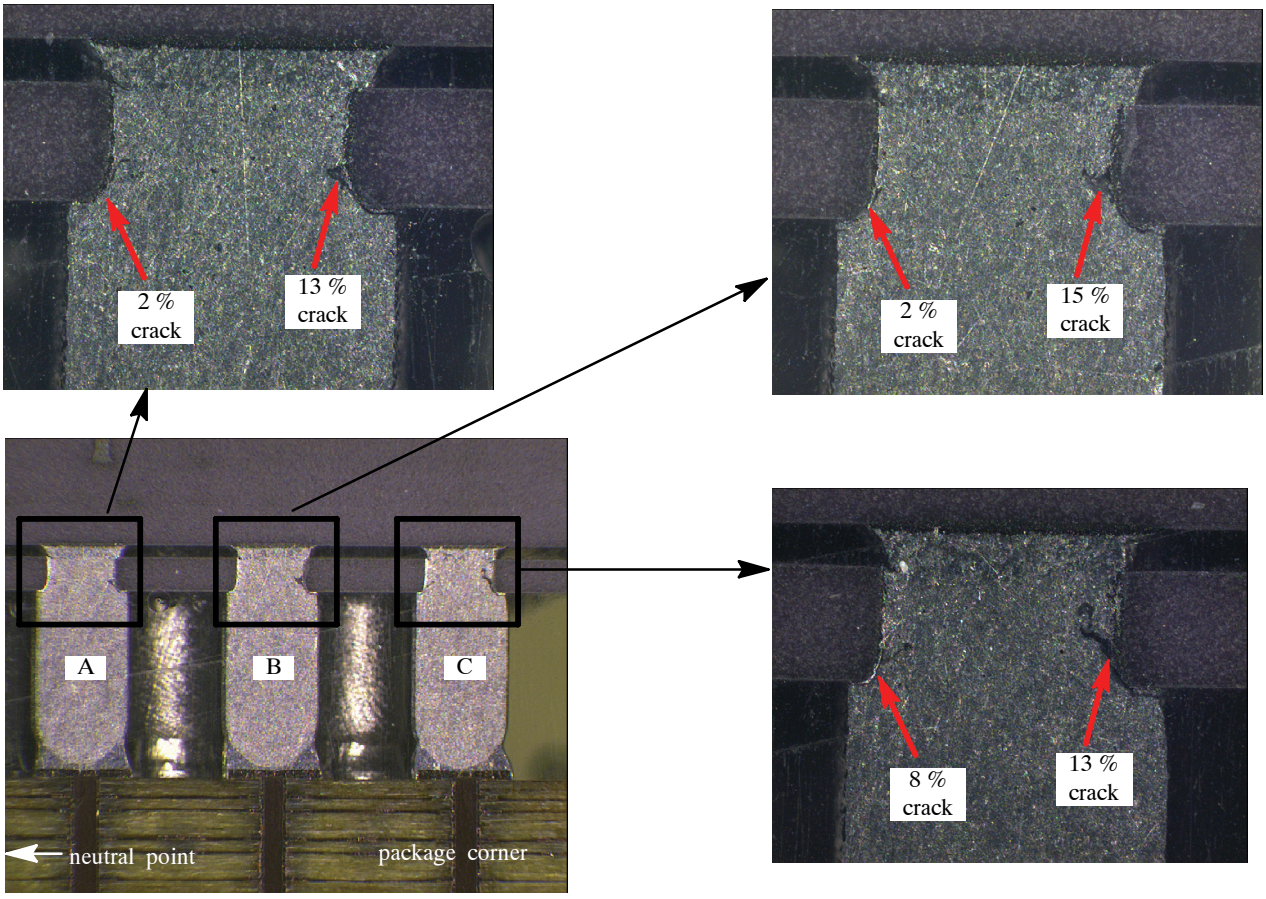
Figure 50: Microsection of a CGA showing a crack



Two micro cracks are located in the column insertion to the cartridge.

The extension of the two micro cracks is estimated at 30 % and 10 % of the column diameter, respectively. The total length of the micro cracks in the column is 40 % of the column diameter (which is more than the accepted 25 % diametrical crack): Reject

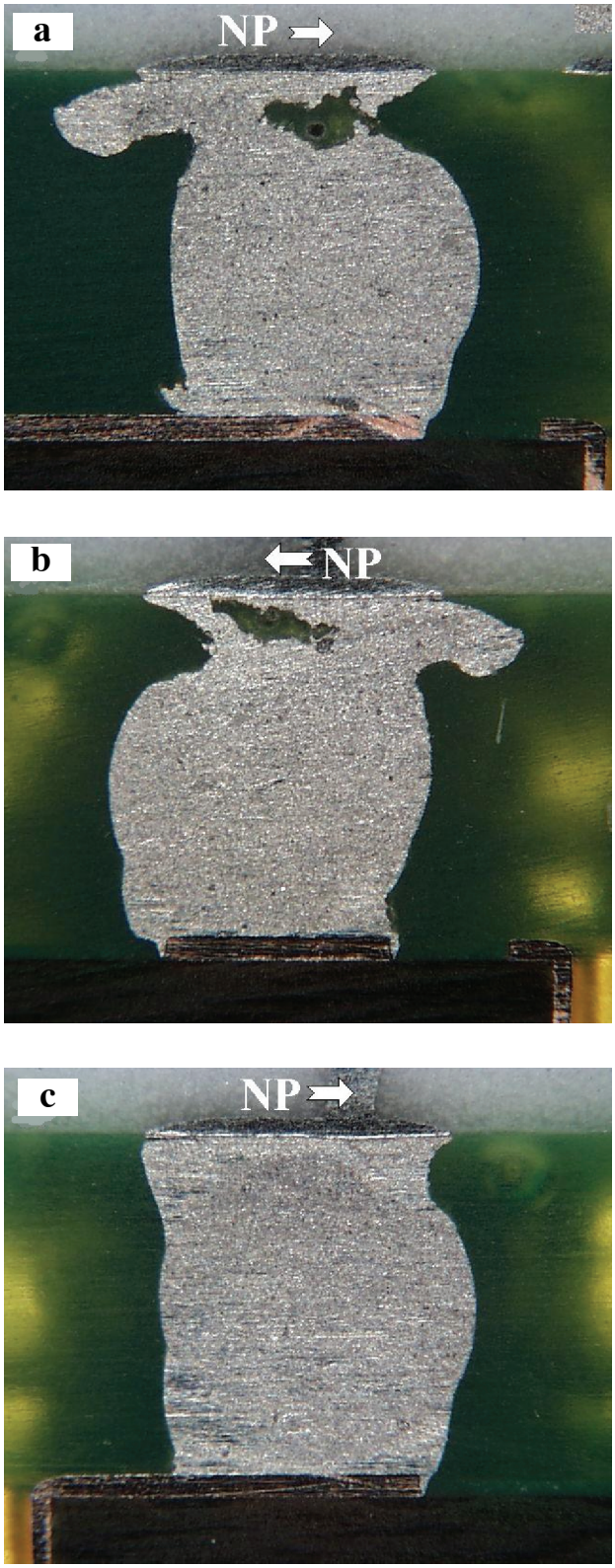
Figure 51: Microsection of CGA showing cracks



Two micro cracks are located in each column insertion to the cartridge. The extents of the micro cracks are estimated at 15 % of column diameter A, 17 % of column diameter B, and 23 % of column diameter C. The crack extensions are lower than the accepted 25 % diametrical crack. Column A-C: ACCEPT

Note that the largest cracks are located at the column sides closest to the package corner.

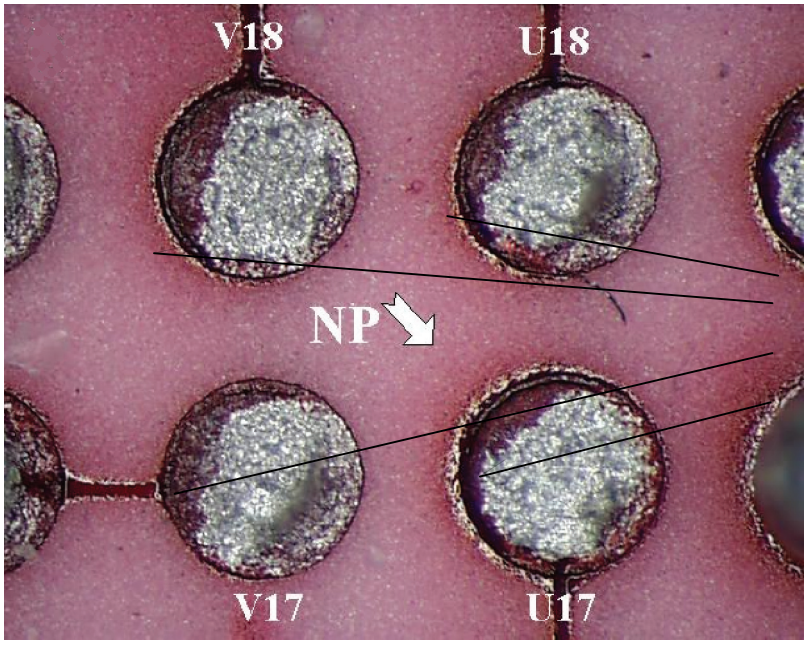
Figure 52: Microsection of CGA showing cracks



(a) (b) Micro sections where cracks are located at the solder joint between solder ball and component pad on the package side. The extent of the cracks is above 50% of the ball diameter: REJECT
(c) Micro section after verification test without any micro cracks: ACCEPT

(The arrows show the direction to the neutral point at the centre of the CBGA)

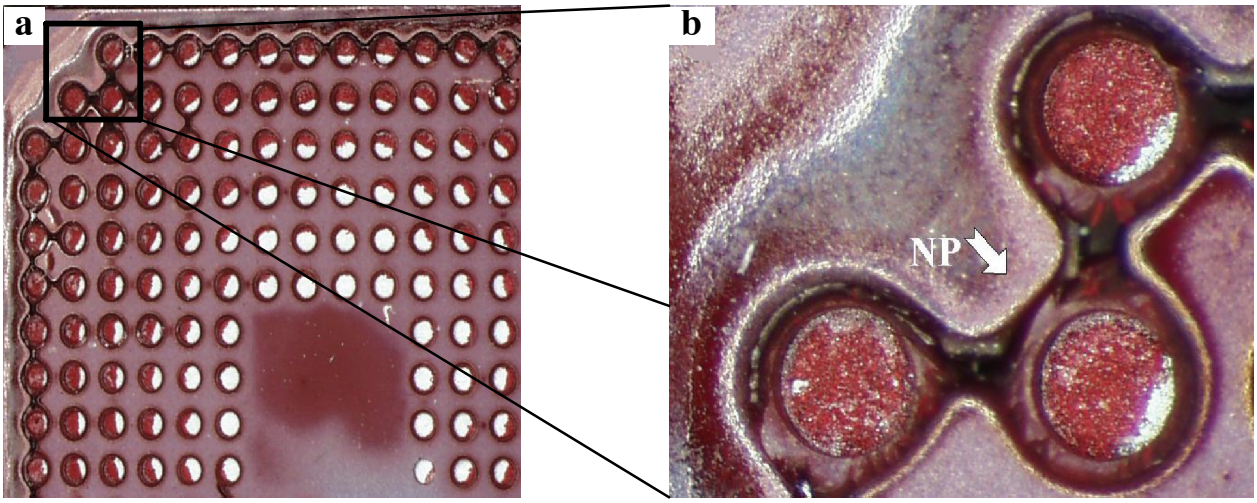
Figure 53: Microsection of CGA showing cracks



The figure shows dye penetration on the component pads on a CBGA package. The interconnections remain on the PCB. The penetrant dye has darkened the area where cracks have been localised after verification testing.
The darkened area is less than 25 % of the total cross sectional area of the original solder joint area: ACCEPT

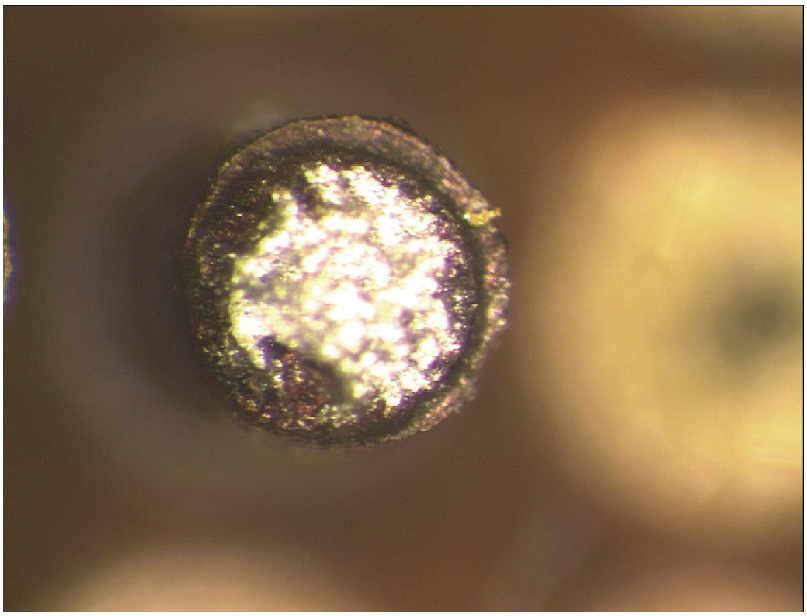
(The arrow shows the direction to the neutral point (NP) at the centre of the CBGA)

Figure 54: Micrography of CBGA after dye penetration testing



(a) The figure shows remaining interconnections on the PCB after the dye penetrant test. The majority of solder joints were severely cracked close to the component pads after the verification test.
(b) The close-up figure clearly reveals the cracks, which extend more than 25 % of the solder balls: REJECT
(The arrow shows the direction to the neutral point (NP) at the centre of the CBGA)

Figure 55: Micrography of CBGA after dye penetration testing



Dye penetrant on a ruptured column. The rupture of the column is localised in the solder joint between the component pad and the column. The dye penetrant has darkened the area where a crack has been localized after verification test. The darkened area is more than 25% of the total cross section area of the column: REJECT

Figure 56: Micrography of a column of CBGA after dye penetration testing

Annex A (informative)

Verification approval

A.1 General

a. The final customer makes the final decision to grant verification status to the supplier of surface mount technology on the basis of examination and acceptance of the fully documented verification test report.

b. The verification test results are compiled by the supplier into a test report data package and contains the results for all the tests specified in clause 14.

c. At this point the surface mount manufacturing processes are established and frozen and documented in a process identification document (PID) in accordance with clause 5.

A.2 Methodology of approval

A.2.1 Request for verification

a. The verification of any SMT assembly is restricted to those suppliers that have been selected to supply equipment for space projects.

b. Each supplier assigns a contact person to be the single point contact for all SMT matters.

c. The following items are submitted to the approval authority.

1. A letter from the supplier addressed to the approval authority, describing his experience in SMT and making the request for verification. The letter is signed by the contact person and the quality assurance manager of the supplier.
2. A process identification document and product control record relating to the technology sample.
3. One technology sample of SMT of the highest possible quality, taken from the assembly line to be verified, not carrying conformal coating (even if the assembly line normally applies conformal coating) is submitted to the approval authority for inspection purposes.

NOTE The reason for not carrying conformal coating is that the sample is inspected.

A.2.2 Technology sample

The technology sample is inspected at by the approval authority based on the criteria set out in clause 13.

EXAMPLE For example, visual inspection can determine the cleanliness and workmanship standard. Metallography can be used to evaluate the SMT connections.

A.2.3 Audit of assembly processing

a. The approval authority informs the supplier of the result of this examination and advises either acceptance or rejection with the start of the next stages of the approval process.

b. The audit assembly process is organized during operation of the SMT processes.

c. The contact person submits the following documents to the approval authority, prior to or during the audit:

   1. Organigram of the company related to the SMT and the quality control functions.
   2. A list of SMT components and connection types, printed circuit board type, staking compounds and conformal coating to be verified.
   3. A description of test capabilities, for example for thermal cycling, vibration, cleanliness testing and metallographic inspection.
   4. A list of personnel who are trained and certified for SMT soldering processes.

d. The findings of the audit remain confidential to the approval authority, but a summary report may be issued.

   NOTE A typical Audit Report questionnaire is shown in Annex D.

A.2.4 Verification programme

a. A verification programme is submitted to the approval authority for acceptance prior to the start of assembly of the test SMT.

   NOTE At the time of the audit specified in A.2.3, details of the verification programme can be discussed. See also clause 14.

b. The number of devices per SMT configuration is at least 3, of which one or more is a repaired configuration.

c. The devices are assembled to the Surface Mount Verification board as specified in subclause 14.1.

   NOTE The number of test samples per SMT configuration can be reduced if justification exists. Such justification can be, for example, that the supplier demonstrates that certain devices can be verified by similarity (see subclause A.2.5).

d. During the environmental test programme, continuous monitoring, by means of an event detector able to detect events of 1 μs (during the last 5 thermal cyclings), of the connections by electrical continuity measurements is preferably applied.

e. After the environmental test programme, analysis of the SMT configurations includes metallography of the worst case connections.

   NOTE d. and e. above are due to the fact that some induced cracks and failures in connections are not apparent visually.

f. A comprehensive qualification test report is compiled and submitted to the approval authority by the supplier.

g. An SMT summary table is submitted with the report.

NOTE Self explanatory examples are presented in Annex B.

A.2.5 Verification by similarity

Several families of SMDs are produced having a wide variation in outline dimensions. The selection of SMDs that is submitted for assembly to printed circuit boards and later to the environmental testing prescribed in clause 14 of this standard does not mean that every size variant is verification tested.

As a result of the large amount of data obtained during past surface mount technology verification programmes, it is proposed that only the largest and smallest SMDs belonging to individual families be selected for testing. The smallest devices ensure that the processing methods are sufficiently dextrous (i.e. their small size can cause handling or soldering problems). The largest sizes ensure that thermal fatigue and vibration fatigue do not cause failures.

Due to the very high cost of some space qualified SMDs consideration can be given to using commercial quality devices and empty packages (specially with internal “daisy–chained” electrical continuity).

(This page is intentionally left blank)

Annex B (informative)

Examples of SMT summary tables

The following Figures present examples of summary tables for different types of components verified against the requirements of this Standard.

Summary table for SMD components verified to ECSS-Q-70-38A by "Name of company"

1) **Assembly Processes:** Vapour phase (VP) and Hand Soldering (HS)
2) **Process Identification Document (PID)**: _____
3) **Solder type:** Wire Sn63 (HS) and Solder paste Sn62 (VP)
4) **Conformal coating:** _____

SMD class	**SMD type**	**Body dimension** (mm)	**Diagonal dimension** (mm)	**Board class** (ΔT=155 °C)	**Company verification report reference**
Resistor ceramic	RM1005 RM2512	2,8 × 1,4 6,35 × 3,18	3,1 7,1	Polyimide Class 1	
Capacitor ceramic	CC0805 CC1812 CC2220	2,3 × 1,45 5,0 × 3,6 6,2 × 5,5	2,7 6,1 8,3	Polyimide Class 1	
Tantalum capacitor	CWR09 D CWR09 H	3,8 × 2,5 7,2 × 3,8	4,5 8,1	Polyimide Class 1	
Tantalum capacitor	CTC-1B CTC-1F	4,2 × 1,7 6 × 3,8	4,5 7,1	Polyimide Class 1	
Diode	MELF A	5,05 × 2,62	5,7	Polyimide Class 1	
Diode	DO213AB	5,2 × 2,7	5,8	Polyimide Class 1	
Ceramic transistor	SMD0.5	10,3x7,64	12,6	Polyimide Class 1	
LCC	3 I/O	3,25 × 2,75	4,3	Polyimide Class 1	
J LCC	28 I/O 68 I/O	11,7 × 11,7 24,4 × 24,4	16,5 34,5	Polyimide Class 1	
CQFP(1)Pitch 1,27 Top brazed	24 I/O	9,4 × 9,4	13,3	Polyimide Class 1	
Flat-pack(2) Pitch 0,65	36 I/O 48 I/O	16,2 × 16,2 16,3 × 10,2	22,63 19,17	Polyimide Class 1	
Plastic component manufacturer X	TSOP54	22,6 × 10,2	24,8	Polyimide Class 1	
Connector	MHD 300			Polyimide Class 1	

(1) Bonded on corner with: _____
(2) Bonded on side with: _____

Name of the Company person responsible: _____ Date: _____ Signature _____

Name of the Final Customer responsible: _____ Date: _____ Signature _____

Summary table for SMD components verified to ECSS-Q-70-38A by "Name of the company"

1) **Assembly Processes:** Vapour phase (VP) and Hand Soldering (HS)
2) **Process Identification Document (PID):** _____
3) **Solder type:** Wire Sn63 (HS) and Solder paste Sn62 (VP)
4) **Conformal coating:** _____

SMD class	**SMD type**	**Body dimension** (mm)	**Diagonal dimension** (mm)	**Board class** (ΔT=155°C)	**Company verification report reference**
Resistor ceramic	RM1005 RM2512	2,8 × 1,4 6,35 × 3,18	3,1 7,1	Polyimide with Cu/Mo/Cu Class 5	
Capacitor ceramic	CC0805 CC2220	2,3 × 1,45 6,2 × 5,5	2,7 8,3	Polyimide with Cu/Mo/Cu Class 5	
Tantalum capacitor	CTC-1B CTC-1F	4,2 × 1,7 6 × 3,8	4,5 7,1	Polyimide with Cu/Mo/Cu Class 5	
LCC	3 I/O 20 I/O	3,25 × 2,75 10,94 × 7,52	4,3 13,27	Polyimide with Cu/Mo/Cu Class 5	
J LCC	28 I/O 68 I/O	11,7 × 11,7 24,4 × 24,4	16,5 34,5	Polyimide with Cu/Mo/Cu Class 5	

Name of the Company person responsible: _____ Date: _____ Signature _____

Name of the Final Customer responsible: _____ Date: _____ Signature _____

Summary table for SMD components verified to ECSS-Q-70-38A by "Name of the company"

1) **Assembly Processes:** Hand Soldering (HS)
2) **Process Identification Document (PID):** _____
3) **Solder type:** Wire Sn63 (HS)
4) **Conformal coating:** None

SMD class	**SMD type**	**Body dimension** (mm)	**Diagonal dimension** (mm)	**Board class** (ΔT=155°C)	**Company verification report reference**
Transistor	CFY67-08	4,2 × 4,2	6,9	Duroid 6002 Class 1	
Schottky Diode	BAS70-71(ES) T1	12,15 × 1,45	12,2	Duroid 6002 Class 1	
Resistor ceramic	RM0805 RM1010	2,03 × 1,27 2,54 × 2,54	2,5 3,6	Duroid 6002 Class 1	
Chip inductor	MPCI-10000 MPCI-20000	2,67 × 2,79 4,2 × 3,94	3,9 5,6	Duroid 6002 Class 1	

Name of the Company person responsible: _____ Date: _____ Signature _____

Name of the Final Customer responsible: _____ Date: _____ Signature _____

Summary table for SMD components verified to ECSS-Q-70-38A by "Name of the company"

1) **Assembly Processes:** Hand Soldering (HS)
2) **Process Identification Document (PID):** _____
3) **Solder type:** Wire Sn63 (HS)
4) **Conformal coating:** _____

SMD class	**SMD type**	**Body dimension** (mm)	**Diagonal dimension** (mm)	**Board class** (ΔT=155°C)	**Company verification report reference**
Resistor ceramic	RM1005 RM2512	2,8 × 1,4 6,35 × 3,18	3,1 7,1	Thermount® polyimide Class 3	
Capacitor ceramic	CC0805 CC2220	2,3 × 1,45 6,2 × 5,5	2,7 8,3	Thermount® polyimide Class 3	
Tantalum capacitor	CTC-1B CTC-1F	4,2 × 1,7 6 × 3,8	4,5 7,1	Thermount® polyimide Class 3	
J LCC	28 I/O 68 I/O 100 I/O	11,7 × 11,7 24,4 × 24,4 34,5 × 34,5	16,5 34,5 48,8	Thermount® polyimide Class 3	
Chip inductor	MPCI-10000 MPCI-20000	2,67 × 2,79 4,2 × 3,94	3,9 5,6	Thermount® polyimide Class 3	
INDU cer/plast	SESI 9.1	10,1 × 10,4	14,5	Thermount® polyimide Class 3	
Capacitor Tantalum(1)	PM94S-4	18,3 × 16,9	24,9	Thermount® polyimide Class 3	
Area Grid Array	CCGA 472 50 mil	29 × 29	41,0	Thermount® polyimide Class 3	

(1) Bonded on side with: _____

Name of the Company person responsible: _____ Date: _____ Signature _____

Name of the Final Customer responsible: _____ Date: _____ Signature _____

(This page is intentionally left blank)

Annex C (informative)

Soldering of area array devices

C.1 General

Only the outer row of solder joints to area array devices can be visually inspected. Inner rows of solder joints cannot be inspected unless X-ray or X-ray-like techniques are used but, even using such techniques, it can be difficult to assure the quality of the solder joints. Reliability of solder joints to area array devices can only be assured by good process control.

Since it is difficult to rework a single solder joint to an area array device, reworking of solder joints generally necessitates that the whole component is removed.

C.2 Solder joint requirements

C.2.1 General requirements

a. Requirements in subclauses 11.5.1 and 13.2 apply to area array devices.

b. The rejection criteria specified in 13.3 apply to area array devices.

NOTE The general requirements of solder joints to reflow soldered components specified in subclause 11.5.1 and 13.2, and the rejection criteria specified in subclause 13.3, also apply to area array devices, although it can be difficult to verify through inspection that the requirements are met.

C.2.2 Voids

C.2.2.1 Overview

Voids are often found to varying extents in solder joints to area array devices. They can be found adjacent to the PCB solder pad and to the device solder pad. For BGAs with eutectic solder balls, they can also be found within the main body of the solder joint. Voids can impact reliability by weakening the solder balls and by reducing the heat transfer and current-carrying capability. However, there are no industry data indicating that voids in the solder joint are a reliability concern unless the voids are very large. In fact, moderately sized voids can cause a slight increase in the solder joint fatigue life. Still, the presence of voids is an indication of the necessity of adjusting the manufacturing parameters.

C.2.2.2 Provisions

a. For voids within the ball refer to Table 9 of subclause 11.5.8.

b. For voids at a solder pad interface refer to Table 9 of subclause 11.5.8.

C.2.3 Solder fillets to high temperature balls

C.2.3.1 Overview

Eutectic solder balls to BGAs completely reflow during the soldering process. That is, the solder in the solder paste and the solder in the ball are blended making up the final joint. This is in contrast to high temperature balls, which do not reflow during the soldering process; see Figure C-1. For this reason, solder joints with eutectic balls have a very different structure compared to solder joints with high temperature balls. Whereas the solder paste volume printed on the solder pads on the PCB has little influence on the geometry of the solder joints for eutectic solder balls, as long as proper wetting occurs, it does have a large impact on the geometry of the solder joints for high temperature solder balls. Too much solder paste increases the risk of bridging between the solder joints, whereas too little solder paste results in meagre solder joints having a reduced fillet diameter between the solder pad and the solder ball. Even a slightly reduced fillet diameter can have a large impact on the fatigue life of the solder joint [6].

C.2.3.2 Provisions

a. The maximum and minimum solder paste volume to be printed on the solder pads for a BGA device is specified.

b. The volume of solder paste printed on the solder pads is verified before the BGA device is mounted on the PCB.

NOTE This is because it is very difficult to detect meagre solder joints even using X-ray inspection techniques.

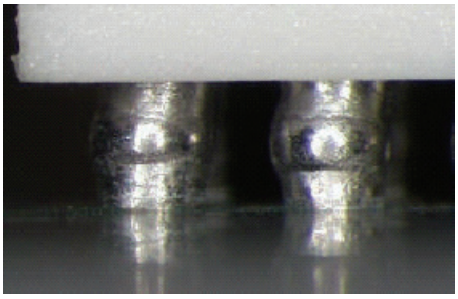


Figure C-1: Typical CBGA solder joint (high melting point balls)

C.2.4 Solder fillets to solder columns

a. The solder completely fills under the column and forms a fillet that wets at least 180 degrees of the column circumference.

b. Avoid excess solder paste since it can increase the fillet height and make the column stiffer resulting in a shorter fatigue life.

NOTE The final solder joint to a solder column often has an asymmetrical fillet with the columns aligned to the edge of the solder pads. This also causes the columns to be tilted (Figure C-2), sometimes in different directions. This is normal and acceptable. It occurs even if the columns are centred in the paste prior to the reflow, and it does not affect the reliability of the solder joint.

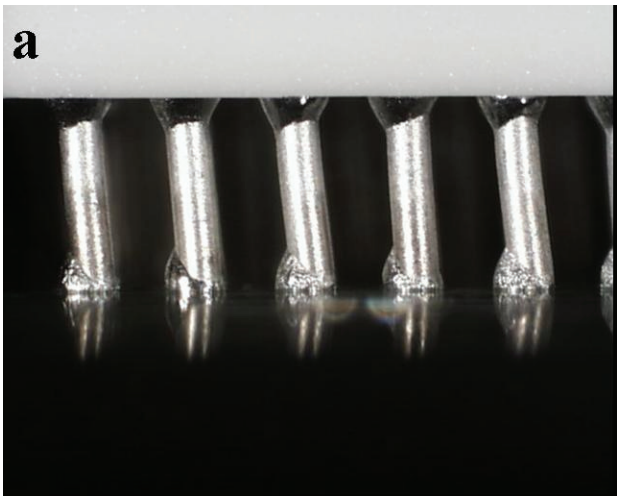


Figure C-2: Tilted columns to a CBGA

C.2.5 Increase of the melting point of solder

C.2.5.1 Overview

During soldering of area array devices with high temperature balls or columns, the eutectic solder used to solder the devices is enriched with lead. This increases the effective melting point of the once eutectic solder. The increased melting point renders reworking more difficult.

C.2.5.2 Provisions

It is good practice to have a solder joint peak temperature of 220 °C with a maximum of 235 °C°. The duration of the solder temperature higher than 183 °C is limited to 145 seconds.

C.2.6 Cold solder

The reflow profile used for soldering area array devices is:

a. specified, and

b. assures that the solder reaches high enough temperature that it wets the pad surfaces for all solder joints and does not leave any cold solder joint.

C.2.7 Brittle fractures

The solder pads on area array devices often have a plating consisting of either electrolytic nickel or electrolytic gold or electroless nickel or immersion gold (ENIG). In both cases, the gold is completely dissolved in the solder during attachment of the balls or columns to the devices. That is, the solder joint is formed towards a nickel surface. Solder joints to electroless nickel surfaces have been found to be much more susceptible to catastrophic, brittle fractures than solder joints to electrolytic nickel and copper surfaces [5]. Analysis indicates that brittle solder joint fracture occurs under a high level of both applied strain and strain rate. The fracture occurs between the nickel surface and the solder, i.e. in the intermetallic layer. Fractures can occur due to thermal shock (too fast cooling after soldering), bending, mechanical shock or thermal cycling (premature failures). This can be related to the black pad embrittlement.

C.3 Removal and replacement of area array devices

C.3.1 General

C.3.1.1 Overview

Removal and replacement are more complicated for grid array devices than for conventional devices because touch-up of individual joints is not feasible [7], [8].

C.3.1.2 Provisions

When removing and replacing area array devices, the whole package is removed and replaced with a new one.

NOTE For this removal, special tooling is used. Most removal and replacement systems are based on a hot-gas reflow tool, although there are also some infrared systems available.

C.3.2 PCB design guidelines for facilitating removal and replacement

a. A clearance of 2 mm to 5 mm for reflow nozzles is left around the perimeter of area array devices to facilitate removal and replacement of the devices.

NOTE The clearance to be left depends on the equipment used for removal and replacement, and the height of adjacent components. The given values are generally used. A large clearance also decreases the risk for reflow of solder joints to adjacent components.

b. If a stencil is used for printing new solder paste, a clearance of 3 mm to 5 mm is used.

c. The assembly is preheated before the hot-gas reflow tool is used.

NOTE 1 This is in order to minimize warpage of the PCB and decrease the stress on the components.

NOTE 2 If a bottom PCB heater is used, it can restrict the type and sizes of components (if any) that can be placed on the corresponding area on the opposite side of the PCB.

d. Capacitors and resistors within the clearance zone are removed and replaced during BGA reworking.

C.3.3 Pre-baking assemblies and devices

a. Assemblies are demoisturized prior to removal and replacement according to ECSS-Q-70-08A, subclause 7.6.

b. If moisture-sensitive devices are used, these are stored and handled according to subclause 8.5.

C.3.4 Device removal

a. Preheating is performed prior to the application of hot gas from the top heater, to a maximum temperature of 10 °C below the T_g for the PCB material.

NOTE This is crucial for minimizing PCB warpage and thermal shock. The higher this temperature is, the better, but without surpassing the limit given in a. above.

b. Each area array device site to be reworked is individually profiled by monitoring the following points: centre and edge joints of the package, adjacent packages, and the PCB.

NOTE Thermal profiling is essential for package removal. Individual profiling is performed due to variations in

adjacent packages and the heat-sinking properties of the PCB internal layers.

c. The hot-gas top heater is used to reflow the solder joints.

d. The joints are profiled to 190 °C minimum (220 °C maximum if the device has high temperature balls or columns) prior to applying the vacuum pick-up force.

NOTE By ensuring that all solder joints are reflowed, lifted PCB pads can be avoided.

e. The temperature of solder joints to adjacent area array devices is limited to less than 150 °C.

f. The flow of hot gas is directed onto to the top of the package.

NOTE Deflection of the gas flow underneath the package tends to create non-uniform solder temperatures across the array pattern.

g. After removal of the package, solder balls remaining on the board and the remaining solder are removed.

NOTE The latter has a high lead content if the devices have high temperature balls or columns and can increase the melting point of new solder paste.

h. It is good practice to limit the growth of copper-tin intermetallics and warping during this process.

NOTE This is the process that presents the greatest risk to the PCB.

C.3.5 Device replacement

For soldering a new package to the board, there are several ways to apply the solder paste, including:

- screen solder paste onto the balls on the area array device,
- screen solder paste onto PCB site,
- solder preforms or decals, and
- dispense solder paste onto PCB site.

The same solder paste volume criteria that apply to initial assembly also apply to replacement processes. For area array devices having eutectic balls, it is possible to just apply a flux to the PCB. However, it is expected to use solder paste, since it increases the stand-off height of the device and thereby also the reliability.

The tooling for reflow soldering of the new package is the same as for package removal. The rework thermal profile has the same limitations as in initial assembly. Too much heat applied causes damage to adjacent packages.

C.4 Inspection techniques

C.4.1 Overview

Inspection methods can be split into non-destructive and destructive methods. Examples of non-destructive methods are visual and X-ray inspections, whereas microsectioning and dye penetrant analysis are examples of destructive methods. Obviously, destructive methods can only be used for qualifying processes, not for quality verification of the final product.

C.4.2 Visual inspection

The traditional method for inspecting solder joints is visual inspection using magnification aids (see subclause 13.1). Although the solder joints to area array components are located beneath the component, visual inspection is still a useful tool for assessing the quality. Basic process control techniques such as PCB

artwork lines around the periphery of the device site indicate accurate placement, and measurement of component height can indicate successful reflow for BGAs with melting balls.

By looking from the side, at least the outer row of solder joints can be inspected. If other components are soldered close to the area array device, it can be necessary to use fibre optics or mirrors (endoscopy) to enable visual inspection of all solder joints in the outer row. Usually, it is possible to see some parts of the solder joints in the rows just inside the outer row and gross defects such as bridges.

C.4.3 X-ray inspection

The most useful non-destructive methods for inspection of solder joints to area array devices are X-ray techniques. X-ray techniques can be split into two main groups: transmission and cross-sectional (laminographic) X-ray techniques. In transmission X-ray, all features in the vertical "line of sight" are viewed concurrently without distinguishing front or back. Differences in material thickness or density result in different transmitted signal attenuations at the detector. With laminography, the X-ray source and the X-ray image plane are moved in a coordinated way with respect to the electronic device being inspected. A clear image of only one layer of the device can thereby be obtained.

Gross defects such as missing solder ball or bridges are easily detected using transmission X-ray techniques. Inadequate reflow of the solder paste and open joints are more difficult to detect, but inspecting the device from an angle can facilitate it. This allows the operator to inspect the shape of the solder connection as it forms onto the pad to verify that the pad is in contact with the solder ball and that the solder is completely wetted to the pad. Inadequate reflow of the solder paste may be seen as a jaggedness around the perimeter of the solder balls.

For BGAs having eutectic solder balls, a tear-drop pad design can improve the identification of open joints or inadequate reflow [9]. If the solder paste is properly reflowed and joined with the solder ball, the solder ball have a distorted shape, which is easily seen in the X-ray image. A tear-drop pad design can be useful also for the inspection of BGAs having high temperature balls and for CGAs, but that has not been verified. Since the balls and columns do not reflow for these components, the distortion of the solder joints can be expected to be less pronounced.

Still, for thick ceramic devices, boards with a very large number of layers and components on both side of the board, it can be impossible to inspect all solder joints using transmission X-ray techniques. Laminography techniques can then be a useful tool.

X-ray analysis is the only available non-destructive method for the inspection and detection of void in solder joints to area array devices. However, it is important to use this technique with caution. Many real time X-ray inspection systems have an X-ray imaging device that exhibits an aberration called "Voltage Blooming" [5]. The result is that the size of a void is affected by the voltage applied to the X-ray source. If the system has this type of aberration, a calibration is done by taking images of solder joints with voids having known sizes.

C.4.4 Microsectioning of solder joints

a. Destructive methods are used to verify the integrity of solder joints to these devices after verification testing.

   NOTE Cracks in solder joints to area array devices are usually very difficult to detect using visual and X-ray inspection techniques.

b. The sample is moulded in a resin to alleviate chipping or destruction of the sample during microsectioning.

c. The resin has an added fluorescent agent.

NOTE This facilitates the detection of fine cracks in solder joints, but also in the PCB laminate.

C.4.5 Dye penetrant analysis

a. Dye penetrant analysis is used as follows to analyse the integrity of the solder joints after verification testing.

1. A low viscosity dye is applied to the sample, which penetrates any cracks or delaminated areas.
2. The dye is dried and the device is then removed, either by prying it away or by applying a pulling force at room temperature or higher.
3. The presence of dye on a solder pad indicates that a crack has been formed prior to the application of the dye. Cracks present in the PCB laminate beneath solder pads are also be coloured with the dye. Thus, coloured surfaces beneath solder pads that are ripped off during the removal of the device indicate the presence of laminate cracks after the verification testing.

   NOTE For further details, see reference [5].

C.5 Verification testing

Due to the lack of stress relief on area array devices, thermo-mechanical stresses are more effectively transferred into the device and the PCB laminate. This can cause cracking of conductors connecting the solder pads, of the PCB laminate and within the device. Such cracking can be cause for rejection. Cracking of the PCB laminate beneath solder pads improves the fatigue life of the solder joints since it makes the joint more flexible. Therefore, it can lead to an overestimation of the fatigue life. That is, the fatigue life can be shorter under more benign conditions that do not cause cracking of the PCB laminate.

C.6 References

(This page is intentionally left blank)

Annex D (informative)

Example of an SMT audit report

CONFIDENTIAL once completed

ECSS-Q-70-38A: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 1	COMPANY DETAILS			
1. NAME				
2. ADDRESS				
3. TEL				
4. FAX				
5. MANAGING DIRECTOR				
6. QUALITY MANAGER				
7. PRODUCTION MANAGER				
8. SMT CONTACT PERSON				
9. SMT PRODUCT RANGE AND HISTORY (brief summary)				
10. Numbers of SMT operators		Design Engineers		QA

ECSS-Q-70-38A: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 2	QUALITY SYSTEM				
1. QUALITY MANUAL* Reference: Issue: Date:				Viewed:	Y N
2. ORGANISATION OF THE QUALITY DEPARTMENT FOR SMT					
3. INTERNAL QUALITY AUDIT SYSTEM Reference: Date of last audit: Comments:				Viewed:	Y N
4. NON-CONFORMANCE SYSTEM Reference:					
	No. of NCRs in previous 12 months:		No. open at audit date:	Viewed:	Y N
5. CURRENT QUALITY APPROVALS Date of last assessment					
6 COMMENT ON COMMITMENT TO ECSS-Q-70-38A					
7. REFERENCE TO GENERAL ESA AUDIT DATE:					

* Note: Request that a copy of the Contents List of the Quality Manual be appended to this report (See Attachment 1).

CONFIDENTIAL once completed

ECSS-Q-70-38A: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 3	PROCESS CONTROL
1. SMT APPROVED (if any) Make reference to an existing list of SMT configurations considered already tested. Identify how the SMT was tested.	

2. Make reference to the procedures that have the following functions and identify current issue and date:

1. Process instructions		Viewed:	Y N
2. Workmanship acceptance/rejection criteria		Viewed:	Y N
3. Calibration of SMT tooling		Viewed:	Y N
4. Control of limited shelf-life materials		Viewed:	Y N
5. Material procurement control with CofC or CofTest		Viewed:	Y N

3. TRAINING Make reference to the procedure for operator and inspector training. Identify the number of certificated operators and inspectors.	Viewed:	Y N	Certificates viewed:	Y N	

ECSS-Q-70-38A: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

CHECK LIST			
1. Components storage and kitting area.		2. Solder paste dispensers	
3. Cleanliness in assembly areas		4. Hand Soldering iron (280°C to 340°C max)	
5. Calibration		6. Degolding bath (250 °C - 280 °C) Pretinning (210 °C - 260 °C)	
7. Lighting (min 1080 lux)		8. Is the soldering equipment well controlled (temperature-time profile, speed control…)	
9. ESD protection and control		10. SMT Assembly Traveller (operator activities, inspector stamps)	
11. Humidity and temperature control		12. Cleaning Equipment	
13. Magnification aids		14. Cleaning Solvent is:	
15. Fume exhaust facilities		16. Cleanliness Testing (< 1,6 µg/cm^2)	

17. PCB drying ovens and procedure		18. Conformal Coating used	
19. Cleanliness in conformal coating facilities		20. Staking compounds/ Adhesives used:	
21. Refrigerators: check expiration dates for staking compounds, conformal coatings		22. Bending tools	
23. Solder alloys used		24. Areas for Nonconforming Items (Quarantine)	
25. Solder fluxes (internal and external) used		26. Laboratories exist for: Temperature cycling Vibration Electrical testing Metallography	

END OF SECTION 4

CONFIDENTIAL once completed

ECSS-Q-70-38A: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 5 DRAFT SUMMARY TABLE (see also Annex B)

1) **Assembly Processes:** _____
2) **Process Identification Document (PID):** _____
3) **Solder type:** _____
4) **Conformal coating:** _____

SMD class	**SMD type**	**Body dimension** (mm)	**Diagonal dimension** (mm)	**Board class** (ΔT=155°C)	**Company verification report reference**

* Adhesive

CONFIDENTIAL once completed

ECSS-Q-70-38A: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 6 FINAL ASSESSMENT

AN ASSESSMENT OF THE SURFACE MOUNT TECHNOLOGY LINE AT THE FOLLOWING SUPPLIER'S FACILITY HAS BEEN UNDERTAKEN AND THE FOLLOWING CONCLUSIONS MADE:

Supplier:

Address:

THE FACILITIES FOR THE ASSEMBLY OF SURFACE MOUNT TECHNOLOGY (ACCORDING TO ECSS Q-70-38 AT THE ABOVE SUPPLIER'S SITE ARE CONSIDERED:

SUITABLE CONDITIONALLY SUITABLE NOT SUITABLE

SUMMARY OF FINDINGS/CONDITIONS OF APPROVAL/SUMMARY OF CORRECTIVE ACTIONS NECESSARY:

NAME SIGN

PROCESS ASSESSMENT CARRIED OUT BY APROVAL AUTHORITY:

IN PRESENCE OF (SUPPLIER):

DATE:

END OF SECTION 6

Annex E (informative)

Additional information

E.1 X-Ray inspection equipment (to 6.8.7)

Various X-ray inspection equipment is available for the non-destructible inspection of SMD joints that are hidden beneath packages. This includes perpendicular transmission, angled transmission and automatic X-ray laminography systems.

X-ray inspection techniques and detectable defects are described in ESA STM-261 [1].

E.2 Melting temperatures and choice

Table E-1: Guide for choice of solder type

Solder type	**Melting range** (°C)		**Uses**
	Solidus	Liquidus	
63 tin solder (eutectic)	183	183	Soldering printed circuit boards where temperature limitations are critical and in applications with an extremely short melting range. Preferred solder for surface mount devices.
62 tin silver loaded	179	190	Soldering of terminations having silver and or silver palladium metallization. This solder composition decreases the scavenging of silver surfaces.
60 tin solder	183	188	Soldering electrical wire/cable harnesses or terminal connections and for coating or pretinning metals.
96 tin silver (eutectic)	221	221	Can be used for special applications, such as soldering terminal posts.
75 indium lead	145	162	Special solder used for low temperature soldering process when soldering gold and gold-plated finishes. Can be used for cryogenic applications.
70 indium lead	165	175	For use when soldering gold and gold-plated finishes when impractical to degold.
50 indium lead	184	210	This solder has low gold leaching characteristic.
10 tin lead	268	290	For use in step-soldering operations where the initial solder joint must not be reflowed on making the second joint (e.g. CGA columns, connections internal to devices)

(This page is intentionally left blank)

Bibliography

[1] ESA STM-261 *An Investigation into Ball Grid Array Inspection Techniques.*

[2] ESA STM-265 *Evaluation of Thermally Conductive Staking Compounds during the Assembly of Spacecraft Electronics.*

[3] ESA SP-1173 *Evaluation of Conformal Coating for Future Spacecraft Applications.*

[4] ESA STM-266 *Assessment of the Reliability of Solder Joints to Ball and Column Array Packages for Space Applications*

[5] IPC-7095, *Design and Assembly Process Implementation for BGAs, IPC, August 2000.*

[6] P.-E. Tegehall and B. D. Dunn, *Impact of Cracking Beneath Solder Pads in Printed Board Laminate on Reliability of Solder Joints to Ceramic Ball Grid Array Packages, ESA STM-267, ESA Publications Division, Noordwijk, 2003.*

[7] P.-E. Tegehall And B.D Dunn, *Assessment of the Reliability of Solder Joints to Ball And Column Grid Array Packages for Spece Applications, ESA STM-266, ESA Publications Divisions, Noordwijk, 2003.*

[8] P. Wood and H. Rupprecht, *BGA and CSP Rework: What is involved? K. Gilleo (Ed.) Area Array Packaging Handbook, McGraw-Hill, Inc., 2001, Chapter 19.*

[9] M. Wickham, C. Hunt, D.M. Adams and B.D. Dunn, *An Investigation into Ball Grid Array Inspection Techniques, ESA STM-261, ESA Publications Divisions, Noordwijk, 1999.*

[10] ECSS-E-10-03, *Space engineering — Testing.*

[11] ECSS-Q-70-22, *Space product assurance — The control of limited shelf-life materials.*

[12] ECSS-Q-70-28, *Space product assurance — Repair and modification of printed circuit board assumblies for space use.*

(This page is intentionally left blank)

ECSS Change Request / Document Improvement Proposal

A Change Request / Document Improvement Proposal for an ECSS Standard may be submitted to the ECSS Secretariat at any time after the standard's publication using the form presented below.

This form can be downloaded in MS Word format from the ECSS Website (www.ecss.nl, in the menus: Standards - ECSS forms).

ECSS Change Request / Document Improvement Proposal

1. Originator's name: Organization: e-mail:				2. ECSS Document number: 3. Date:	
4. Number.	5. Location of deficiency clause (e.g. 3.1)	page (e.g. 14)	6. Changes	7. Justification	8. Disposition

Filling instructions:

1. **Originator's name -** Insert the originator's name and address
2. **ECSS document number -** Insert the complete ECSS reference number (e.g. ECSS-M-00B)
3. **Date -** Insert current date
4. **Number -** Insert originator's numbering of CR/DIP (*optional*)
5. **Location -** Insert clause, table or figure number and page number where deficiency has been identified
6. **Changes -** Identify any improvement proposed, giving as much detail as possible
7. **Justification -** Describe the purpose, reasons and benefits of the proposed change
8. **Disposition -** (Not to be filled in by originator of CR/DIP)

Once completed, please send the CR/DIP by e-mail to: ecss-secretariat@esa.int

(This page is intentionally left blank)