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The capability approval programme for hermetic thick-film hybrid microcircuits

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ABSTRACTS

This specification defines the general requirements for capability approval of a manufacturing line for Hermetic Thick Film Hybrid Microcircuits.

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1. SCOPE

This specification defines the general requirements for capability approval of a manufacturing line for Hermetic Thick Film Hybrid Microcircuits. For procurement requirements, see ESA PSS-01-608.

ESA approval mandate will be exercised upon conclusion of the Evaluation Phase and at the end of the programme.

Before the Evaluation Phase can commence, the manufacturer shall define the capability approval domain by specifying the processes, materials and techniques involved in the technology for which approval is sought.

2. GENERAL

2.1 INTRODUCTION

The manufacturer shall have and implement a quality and reliability programme compatible with this specification. The review of this programme by ESA is part of the capability approval.

The manufacturer shall be responsible for the performance of tests and inspections required by this specification. All of these tests and inspections shall be performed at the plant of the manufacturer and approved by the manufacturer's Quality Assurance organisation. The use of external facilities and/or services is subject to prior ESA approval.

ESA, or its designated representative, reserves the right to participate in, or execute, survey, audits, reviews and source inspections as well as to witness any tests and to have resident or temporary personnel at the manufacturer's plant during the programme period. Participation by ESA, or its designated representative, in any approval activities shall never be considered as substitution for, or release from, the manufacturer's responsibilities.

The manufacturer shall grant personnel of ESA, and/or of its designated representative, free access to any documentation, hardware and facilities listed in the Process Identification Document (PID).

2.2 APPLICABLE DOCUMENTS

The following documents are applicable to the extent specified herein.

ESA PSS-01- 60	Component Selection, Procurement and Control for ESA Spacecraft and Associated Equipment.

ESA PSS-01- 70	Materials and Process Selection and Quality Control for ESA Spacecraft and Associated Equipment,
ESA PSS-01-201	Contamination and Cleanliness Control,
ESA PSS-01-608,	Generic Specification for Hybrid Microcircuits,
ESA PSS-01-702,	A Thermal Vacuum Test for the Screening of Space Materials,
ESA PSS-01-708,	The Manual Soldering of High Reliability Electrical Connections,
ESA PSS-01-716,	The Listing and Approval Procedure for Materials and Processes,
ESA PSS-01-722,	The Control of Limited Life Materials,
MIL-STD-202,	Test Methods for Electronic and Electrical Component Parts,
MIL-STD-883,	Test Methods and Procedures for Microelectronics,
MIL-STD-38510,	Microcircuits, General Specification for,
QRC-06C,	Checklist for Thick Film Hybrid Microcircuit Manufacturers and Line Survey.

2.3 REFERENCE DOCUMENTS

ESA PSS-01-610, Design Guidelines for Thick Film Hybrid Microcircuits.

2.4 DEFINITIONS

The definitions listed in Annex A shall apply.

2.5 ACCESS TO MANUFACTURING FACILITIES

To enable the survey team of ESA, or its delegated representative, to carry out the capability survey and line survey, the manufacturer shall grant free access to the facilities concerned. He shall also enable the team to witness any development, engineering, production and quality assurance operations involved in the processes for which approval is sought.

2.5.1 Checklist

To facilitate the evaluation procedure, ESA will apply Checklist ESA QRC-06C.

2.6 CAPABILITY SURVEY

The purpose of this survey is to assess the following aspects of the manufacturer's organisation:

- General organisation and management,
- Quality and Reliability Assurance organisation, including definition of authority and effectiveness,
- Facilities and capabilities of the plant in which the thick film hybrid microcircuits will be manufactured and tested,
- Nonconformance control.

Before and/or during the actual survey, the manufacturer shall provide ESA with any documentation which may assist the survey team in the execution of its tasks. As a minimum, this documentation shall include:

- An organigram delineating authority, responsibility and interrelationship between Engineering, Production, Quality and Reliability Assurance, Procurement and Management;
- Expertise of all key personnel employed in the Production and Product Assurance Departments;
- A list of contracts with ESA and/or national space agencies for component evaluation and qualification;
- The name(s) and location(s) of any other plant(s) of the manufacturer where electronic parts are produced according to the same, or a similar, technology as applied to the hybrid microcircuits for which qualification is sought;
- A flow-chart and any available procedures relative to the processes and controls applied in the production of the devices to be evaluated and approved.

2.6.1 Organisation and Management

The manufacturer shall clearly define his policy on:

- Authority and responsibility of Quality and Reliability management vis-à-vis general management;
- Support requested by the Research and Development Department from Engineering and/or Quality Assurance personnel;
- Employee motiviation (bonus scheme, incentives, operator training and certification, etc.).

2.6.2 Assessment of Design Rules

For assessment of the design of the Hermetic Thick Film Hybrid Microcircuits, the manufacturer shall provide ESA with the design rules he proposes to apply. General design guidelines are given in ESA PSS-01-610.

2.7 PRODUCT ASSURANCE REQUIREMENTS

2.7.1 Organisation and Responsibilities

The manufacturer shall have an effective Quality and Reliability organisation, suitable facilities and competent Product Assurance personnel with a sufficient degree of independence from the company's design and manufacturing functions to deal objectively with the Product Assurance aspects of the hybrid microcircuits in compliance with the applicable ESA documents.

The Quality and Reliability organisation shall have direct and unimpeded access to higher management, to which it shall report regularly on the status and adequacy of the programme.

The Quality Assurance organisation shall be responsible for the implementation of all requirements of this specification and the execution

of this programme to the satisfaction of the customer. He shall present to the customer only those items/documents which he determines to be in full compliance with those requirements of this and all applicable specifications listed that concern the customer.

2.7.2 Quality and Reliability Requirements

The manufacturer shall establish and implement a Quality and Reliability programme which fully complies with all of the applicable ESA PSS specifications. Special attention shall be paid to:

- Training of operators/inspectors,
- Definition of workmanship standards,
- Reliability engineering activities,
- Configuration Control,
- Quality Assurance activities according to PSS-01-20,
- Materials and Process selection according to PSS-01-70 and PSS-01-716.

2.8 LAY-OUT OF FACILITIES

The manufacturer shall provide ESA with the lay-out of the facilities to be surveyed, showing the location of each production area, the cleanliness standards and dust count frequency applicable to each area and operation, and including a list of equipment, specifying its accuracy and calibration frequency.

2.9 LINE SURVEY

During this survey, which will comprise all aspects of the production line, special attention will be paid to those processes, process steps, materials, piece parts and controls that are involved in the manufacture of the devices concerned. The manufacturer shall demonstrate to ESA the methods evolved on the basis of in-house experience for investigation and optimisation of all processes for which approval is sought.

For the purpose of this survey, the subject test structures will be divided according to the major processes performed in the three main production areas of a hybrid microcircuit manufacturing facility, viz.:

a) **Thick Film Network**

This is often called the pure thick film circuit and requires basically the print and fire technique, resistor trimming, without additions or encapsulation;

b) **Thick Film Hybrid Assembly**

This involves the adding on of chips or other circuits and their connection to the substrate;

c) **Encapsulation or Mounting of Microcircuit**

This involves the encapsulation of the substrate or its mounting onto a base-plate or similar structure.

2.9.1 Production Documents

All documents related to the processes for which capability approval is sought shall be made available to ESA. Any proprietary documents shall be included, but marked as such.

2.9.2 Process Flow-chart (PID)

This chart shall show the sequence of production and inspection steps. Inspections shall include each measurement, test or visual examination performed. The flow-chart shall also show:

- number, issue and revision date of the specification applicable to each production and inspection step;

- department, division or section responsible for each operation involved in the processing, production and quality control;
- point at which statistical control records are applied.

The issue and revision date of the above mentioned documents may be listed separately.

2.9.3 Travelling Documents

The manufacturer shall prepare and use a travelling document for each lot. This document shall show as a minimum:

- lot identification,
- operation,
- date of each operation,
- number in/out at each operation,
- operator identification,
- nonconformance references.

2.9.4 Process Control Chart

The process control chart shall show as a minimum:

- title of relevant process,
- name or code number of station at which it is used,
- lot identification,
- dates recorded,
- number of items inspected,
- identification of equipment adjustment,
- percentage of defective devices,
- average nominal values,
- average limits.

2.9.5 Process Documentation

The manufacturer shall prepare and maintain documents for incoming inspection, production, quality assurance and process control such as specifications and procedures establishing:

- materials and piece parts,
- operations,
- equipment,
- calibration methods,
- measurements,
- tests,
- inspections,
- tolerances.

These documents and any revisions thereof shall be available at all times to operating personnel and, upon request, shown to the evaluating and qualifying authority.

2.9.6 Traceability

The manufacturer shall record the manufacturing data and material history of all units processed according to this specification and maintain these records for a minimum of five years.

2.10 LOCATION OF PROCESSING AREAS

The manufacturer shall specify the location where each of the key processing steps is performed. The evaluating authority shall be notified of any changes in these locations to determine if re-evaluation is required.

2.11 WORK AREAS

2.11.1 General Requirements

The devices concerned shall be produced in a controlled area. This implies that:

- only authorized personnel shall have access to such area and that within such area:
- personnel shall wear protective clothing,
- smoking, drinking and eating shall be prohibited,
- housekeeping shall be according to a written schedule,
- equipment shall be compatible with the cleanliness standard required in the controlled area.

2.11.2 Environmental Control

The manufacturer shall specify for each process step:

- relative humidity,
- temperature,
- particle count.

He shall demonstrate the manner in which these conditions are controlled taking into account the relevant requirements defined in Table 1 and Specification ESA PSS-01-201.

2.12 HANDLING OF SUBSTRATES

The manufacturer shall furnish evidence that adequate provisions are in force for the careful handling and storage of substrates throughout production cycle. Any damage to substrates shall be recorded together with details of the station and/or stage of operation at which the damage occurred.

2.13 PURITY OF MATERIALS

The manufacturer shall keep records to verify that the materials used in production are of a consistent purity level and meet the application requirements.

TABLE 1 - ENVIRONMENTAL REQUIREMENTS

Process Step	Cleanliness Class	Humidity (% RH)	Temperature (°C)
Wet photoresist processes for mask work, etc.	10 000	To be specified by manufacturer	To be specified by manufacturer
Areas where wet printing paste work is performed	10 000	50 ± 5	25 +0 -5
Areas where firing and soldering work is performed	100 000	50 ± 5	To be specified by manufacturer
Semiconductor chip mounting work and wire-bonding manufacturer	10 000	50 ± 5	To be specified by manufacturer
Mounting of encapsulated components on ceramic substrates	To be specified by manufacturer	To be specified by manufacturer	To be specified by manufacturer
Precap visual inspection and final sealing areas	100	50 ± 5	To be specified by manufacturer
Cleaning of "open" circuit types and packaging into sealed plastic bags	10 000	50 ± 5	To be specified by manufacturer
Other process steps	To be specified by manufacturer	To be specified by manufacturer	To be specified by manufacturer

Temperature and humidity shall be controlled and continuously recorded.

Cleanliness class shall be checked regularly during production.

3 EVALUATION PHASE

3.1 GENERAL

The Evaluation Phase shall consist of:

a) Capability Survey

This survey is made to assess a manufacturer's general capability in the production of reliable circuits.

b) Line Survey

This survey consists of an analysis of a manufacturer's technology and production line based on applied processes and controls and a detailed study of all available test data for the identification of critical processes and controls.

c) Evaluation Testing

This involves respectively the selection, production and testing of test structures for determination of their stress limits and weaknesses.

d) Corrective Actions

If, as a result of evaluation testing, the test structures show weaknesses or deficiencies, the manufacturer shall take any corrective actions required by ESA.

e) ESA Approved Capability Domain

After all required corrective actions have been implemented to the full satisfaction of ESA, ESA will approve the manufacturer's

capability domain as defined in the PID at the end of this phase. This approval will enable the manufacturer to start the next phase of the programme.

3.2 EVALUATION TESTING

Evaluation testing shall comprise four sequential steps, viz.:

- Selection of techniques, processes and materials to be certified;
- Based on the selection specified above, manufacture of test structures or circuits;
- Testing of test structures or circuits;
- Evaluation of test results.

3.2.1 Selection of Techniques

On the basis of the processes, materials and techniques proposed by the manufacturer for approval, the manufacturer shall propose the main techniques and type of encapsulation, define the test structures and draw up the test plans in accordance with the requirements of this specification.

Tables 2 and 3 show respectively the possible main techniques and encapsulation or mounting methods. Only certain combinations of main techniques and encapsulation or mounting methods shall be permitted; these are shown in Table 4 together with the type designations of the corresponding test structures.

The manufacturer shall be free to choose which of the different subtechniques applicable to a specific main technique he wishes to use. However, the lay-out and content of the corresponding test structure shall be agreed with ESA. The selection shall be made before commencing manufacture of the test structures. Table 5 lists the various subtechniques.

The manufacturer shall draw up a list of processes and select the raw materials, piece parts and added-on or applied materials, and ascertain their conformance to the design, quality and procurement requirements defined in this specification and ESA Specifications PSS-01-60, PSS-01-70 and PSS-01-608, as relevant. Alternatively, he shall prove their suitability for space application by other documentary evidence.

Each process step shall be chosen solely on the basis of the materials, techniques and controls applied at the time of evaluation. A preliminary Process Identification Document (PID) shall be prepared for the processes and procedure to be applied. The PID shall list all constituent materials and piece parts.

The manufacturer shall ensure that all materials and processes for which certification is sought are adequately covered by the programme. Prior to its implementation, this programme shall be submitted to ESA for approval.

TABLE 2 - MAIN TECHNIQUES

A	General purpose hybrid circuits in 1- or 2-layer technique. Power dissipation: 0.2 W or less per cm^2 substrate. Terminal current : 1 A or less
B	Multilayer hybrid circuits with 3 or more conductor layers. Power dissipation: 0.2 W or less per cm^2 substrate. Terminal current 1 A or less
C	High-power and high-current hybrid circuits for power-supply and power-conditioning circuits etc., with continuous power dissipation more than 0.2 W per cm^2 substrate or terminal currents more than 1 A.
D	High-voltage hybrid circuits, voltage dividers etc. for more than 1000 V.

TABLE 3 - MOUNTINGS AND ENCAPSULATION

Q	Unencapsulated and unmounted substrates
R	Substrate mounted on simple metal-plate structure
S	Substrate mounted in hermetically sealed low-power metal package
T	Substrate mounted in hermetically sealed low-power ceramic package
U	Substrate mounted in hermetically sealed high-power metal package

TABLE 4 - PERMITTED COMBINATIONS OF MAIN TECHNIQUES AND MOUNTING OR ENCAPSULATION METHODS FOR DEFINITION OF TEST STRUCTURES

Main Technique	Mounting or Encapsulation				
	Q	R	S	T	U
A	QA1	RA1	SA1	TA1	Not applicable
B	QB1 and QB2	RB1 and RB2	SB1 and SB2	TB1 and TB2	Not applicable
C	Not applicable	RC1	Not applicable	Not applicable	UC1
D	QD1	RD1	Not applicable	TD1	Not applicable

Example

SA1 is a type A1 test substrate (covering general-purpose low-power hybrid circuitry) mounted in a hermetically sealed low-power metal package.

Definition of Main Techniques: See Table 2.

Definition of Mounting and Encapsulation Methods Q to U: See Table 3.

Definition of Test Substrates A1 to D1: See Table 6.

TABLE 5 - SUBTECHNIQUES

I	1-or 2-layer conductor
II	Multilayer conductor
III	Printed resistors
IV	Protective covering
V	Printed capacitors
VI	Cross-over by wire bonding
VII	Termination with wire-leads
VIII	Mounting of encapsulated components
IX	Mounting of resistor or capacitor chips
X	Mounting of chip-carriers
XI	Chip and wire bonding
XII	Substrate mounting on metal plate
XIII	Substrate mounting in package

3.2.2 Sequence of Operations for Selection, Manufacture and Testing of Test Structures

- The manufacturer shall propose and submit to ESA for approval those processes that he wishes to adopt.
- Joint agreement by ESA and the manufacturer on subtechniques (see Table 5).
  Joint agreement by ESA and the manufacturer on main techniques and mounting or encapsulation methods.
- Preparation by the manufacturer of the applicable documentation and lay-outs of test structures.
- Manufacture and testing of test structures, preparation of report.
  ESA may require to monitor certain tests.
- Destructive Physical Analysis (DPA) of control devices by ESA or an independent test laboratory.

3.2.3 Test Structures for Line Evaluation

The test structures to be manufactured shall:

- be based on the processes selected,
- be such that they are representative of the technology involved,
- be in accordance with the controls, limits and constraints agreed between ESA and the manufacturer,
- meet the requirements of this specification,
- be tested for any weakness, so that restraints of the applied processes and technologies may be determined, and
- take into account any inherent criticalities.

3.2.4 Test Structures and Applicable Test Programmes

Table 6 specifies the test substrates to be used in the manufacture of the different test structures and refers to the paragraphs in which details are described.

Table 7 shows type designations and numbers of test structures to be manufactured for evaluation testing together with the applicable test plans set out in Paragraph 3.2.6.

TABLE 6 - TEST SUBSTRATES AND PROCEDURES

Substrate	Description	Para
A1	Substrate for manufacture of general-purpose low-power hybrid microcircuit:- - 1- or 2-layer printed conductors, - printed resistors, - capacitors and cross-overs, - attachment of terminals, - passive and active components. Applicable subtechniques to be chosen from Table 5.	3.2.5.1
B1	Substrate for multilayer printing techniques	3.2.5.2
B2	Substrate for component attachment on multilayer circuits	3.2.5.2
C1	Substrate for high-power and high-current hybrid technique	3.2.5.3
D1	Substrate for high-voltage hybrid technique	3.2.5.4

TABLE 7 - TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED AND APPLICABLE TEST PLANS

Description Example	Test Structure	No. of Pcs to be manufactured	Test Plan No.	Example
General-purpose low-power hybrid, unencapsulated	QA1	13	1	
General-purpose low-power hybrid, on metal plate	RA1	13	1	
General-purpose low-power hybrid in metal package	SA1	11	2	
Low-power hybrid in ceramic package	TA1	11	2	Mounting or package type definition see Table 3
Multilayer network, unencapsulated	QB1	13	1	
Multilayer network with components attached	QB2	13	1	
Multilayer network on metal plate	RB1	13	1	Q A1
Multilayer network with attached components on metal plate	RB2	13	1	
Multilayer network in metal package	SB1	11	2	Substrate type Definition see Table 6
Multilayer with attached components in metal package	SB2	11	2	

TABLE 7 continued on next page.

TABLE 7 - TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED AND APPLICABLE TEST PLANS (Continued)

Description Example	Test Structure	No. of Pcs to be manufactured	Test Plan No.	Example
Multilayer network in ceramic package	TB1	11	2	See previous page
Multilayer network with attached components in ceramic package	TB2	11	2	
High-power hybrid on metal plate	RC1	13	3	
High-power hybrid in metallic package	UC1	11	4	
High-voltage hybrid, unencapsulated	QD1	13	5	
High-voltage hybrid on metal plate	RD1	13	5	
High-voltage hybrid in ceramic package	TD1	11	6	

3.2.5 Description and Lay-out of Test Substrates

The following paragraphs describe the lay-out of test substrates A, B, C, D and E. As a guideline, the test structures described and illustrated in the following paragraphs have been implemented on 25 x 50 mm substrates. The manufacturer may however choose different dimensions according to the technology for which capability approval is sought.

Any commercially available added-on parts required for assembly shall be as far as possible equivalent to space-qualified parts.

The manufacturer shall adhere to the specified patterns unless the technology involved requires deviation. In such case, the revised drawing of the pattern shall be submitted to ESA for approval.

3.2.5.1 Test Structure A for Low-Power Hybrid Technique

This pattern is illustrated in Figure 1 and specifies printed resistors and conductors, a special pattern of thin lines placed closely together for evaluation of mask and printing quality, positions for attached chip capacitors and active components as well as a pattern for wire and printed crossovers.

With reference to the subtechniques listed in Table 5, only those sections of the pattern that are required shall be implemented.

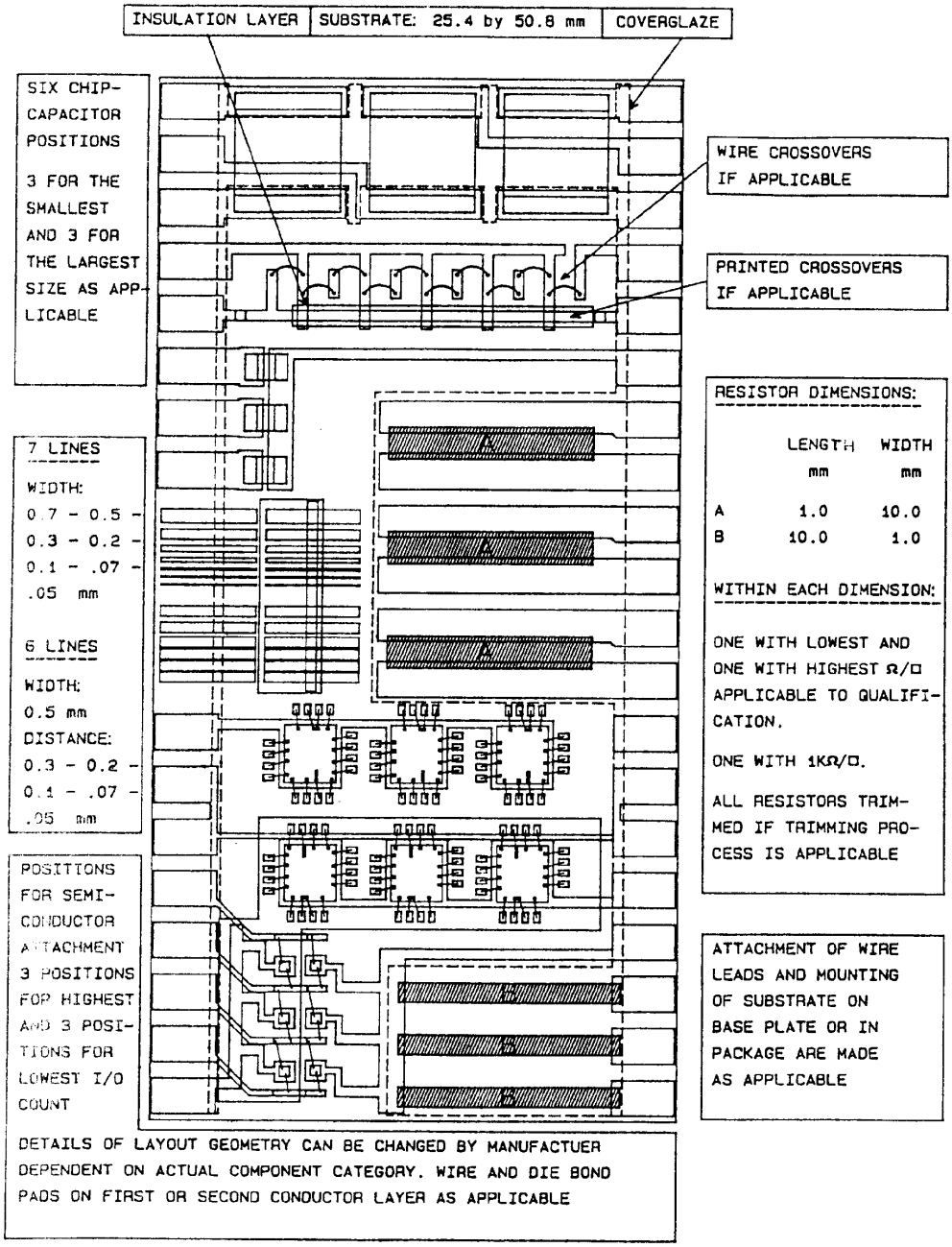


FIGURE 1 - TEST STRUCTURE 'A', GENERAL PURPOSE HYBRID TECHNIQUE

Rules for Endurance Testing

For evaluation purposes, the following rules shall be applied when subjecting Test Structure 'A' to Test No. 5, "Endurance Testing" of Table 8

Thick Film Resistors

'A' Resistors: 0.25 W, maximum 20 V d.c.;
'B' Resistors: 0.25 W, maximum 250 V d.c.,
Load Cycle : 90 minutes on; 30 minutes off.

Semiconductors

No load.

Chip Capacitors

No load.

Printed Capacitors and Cross-overs

100 V d.c., continuous.

Depending on the technology, the substrate may be mounted or unmounted, on a base-plate or in a package.

If applicable, solder leads may be used.

3.2.5.2 Test Structures 'B1' and 'B2' - Multilayer Printing Technique and Component Attachment to Multilayer Circuits

Patterns are illustrated in Figures 2 to 9 inclusive.

a) Test Pattern 'B1' covering Printing Technique

Test Philosophy

The test pattern covers the range of 0.1 to 0.3 mm line widths and distances in combination with a number of conductive layers which may vary between 3 and 8. Before evaluation and capability approval, the manufacturer shall select the number of conductor layers and prepare the test patterns accordingly.

The permitted minimum line width and distance cannot be chosen in advance. The graduated set of lines of the test pattern decreases in width and distance and only the test result will prove the minimum width of the lines which can be achieved by the manufacturer.

Approval is usually granted for the larger line width following the one which passed the printing test without failures.

Line Widths

Generally, line widths and distances less than 0.1 mm are not considered suitable for high reliability space application. Although even 0.1 mm is close to the allowable limit, this width has been included because it will provide evidence of possible limitations of the manufacturer's printing technique. The upper limit of 0.3 mm is considered to be the minimum requirement to be met by a process line intended for the production of multilayer hybrids.

Number of Layers

Also covered by the test pattern are 3 to 8 conductive layers, 1- and 2-layer circuits being covered by type 'A' patterns. In view of the present state of the art, circuits with more than 8 layers are not considered suitable for space application.

Printing Alignment

Printing alignment often creates a problem when feed-throughs have to be made linking the lines of several independent layers, especially when the lines are thin. This problem is reflected by Figure 6, area 2 of Figure 3, showing pairs of lines with decreasing widths running across all layers from bottom to top and back again.

Printing Irregularities Around Feed-throughs

The frequent occurrence of printing irregularities around feedthroughs is due to small misalignments and the differences in thickness of dielectric layers and fill-up dots of conductors.

A similar printing problem may arise when lines and feed-throughs are positioned on top of each other over several layers (see area 3 of Figures 3 and 7).

As the positioning of several feed-throughs directly on top of each other is not only very difficult, but also considered to be bad design practice, the test pattern specifies broken feedthrough lines alternating with straight lines from layer to layer.

Pinholes and Insulation Resistance

Multilayer circuits frequently fail because pinholes or contamination by conductive particles in the dielectric layers result in low

dielectric strength or direct short-circuit between conductive layers. Another problem may be created by some dielectric hygroscopic pastes which must be covered by a glass passivation layer to prevent humidity absorption and reduction of insulation resistance.

Area 1 of Figure 3 and Figure 5 shows how both problems are solved by printing successive metallised areas one over the other.

Lines over Steps

The printing of lines over successive steps is normally avoided and, especially where thinner lines are required, it is good design practice to keep the line at one single level. However, in special cases, wider lines running over steps of insulation layer may be necessary (see Area 1 of Fig. 3 and Fig. 5).

Resistors

Although multilayer hybrids are frequently pure connection patterns for digital integrated circuit chips, some printed resistors may be required. As shown in Figures 3 and 4, these are usually placed on top of the circuit (Area 4).
Five resistors are made using the lowest, and five using the highest, /square paste to be tested. No trimming is permitted of resistors printed on dielectric.

Direction of Printing

Alignment around feed-throughs is often made difficult by stretch in the printing masks as a result of friction during printing. This problem becomes even more complicated when printing is performed perpendicularly to very thin line systems. Unfortunately, it is practically impossible for all printing to run parallel to the lines of a system because some will always be perpendicular to others or at

least at an angle of 45°, depending on the printing technique. For this reason, it is a mandatory requirement that **THE DIRECTION OF PRINTING (IN WHICH SQUEEGEE RUNS) SHALL ALWAYS BE PERPENDICULAR TO, OR AT A 45° ANGLE WITH, THE LENGTH OF THE TEST PATTERN**

Packaging

Depending on the mounting or encapsulation method, test structures may be mounted on a base-plate, unmounted or encapsulated in hermetically sealed packages.

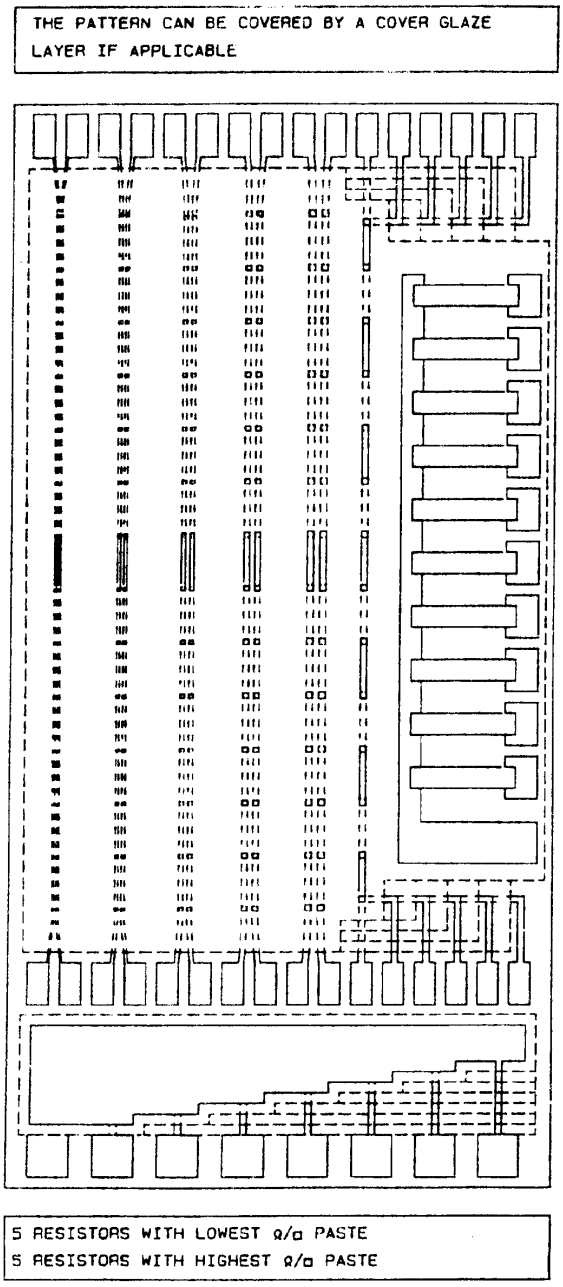


FIGURE 2 - GENERAL LAY-OUT OF PATTERN FOR TEST STRUCTURE B1 - MULTILAYER PRINTING

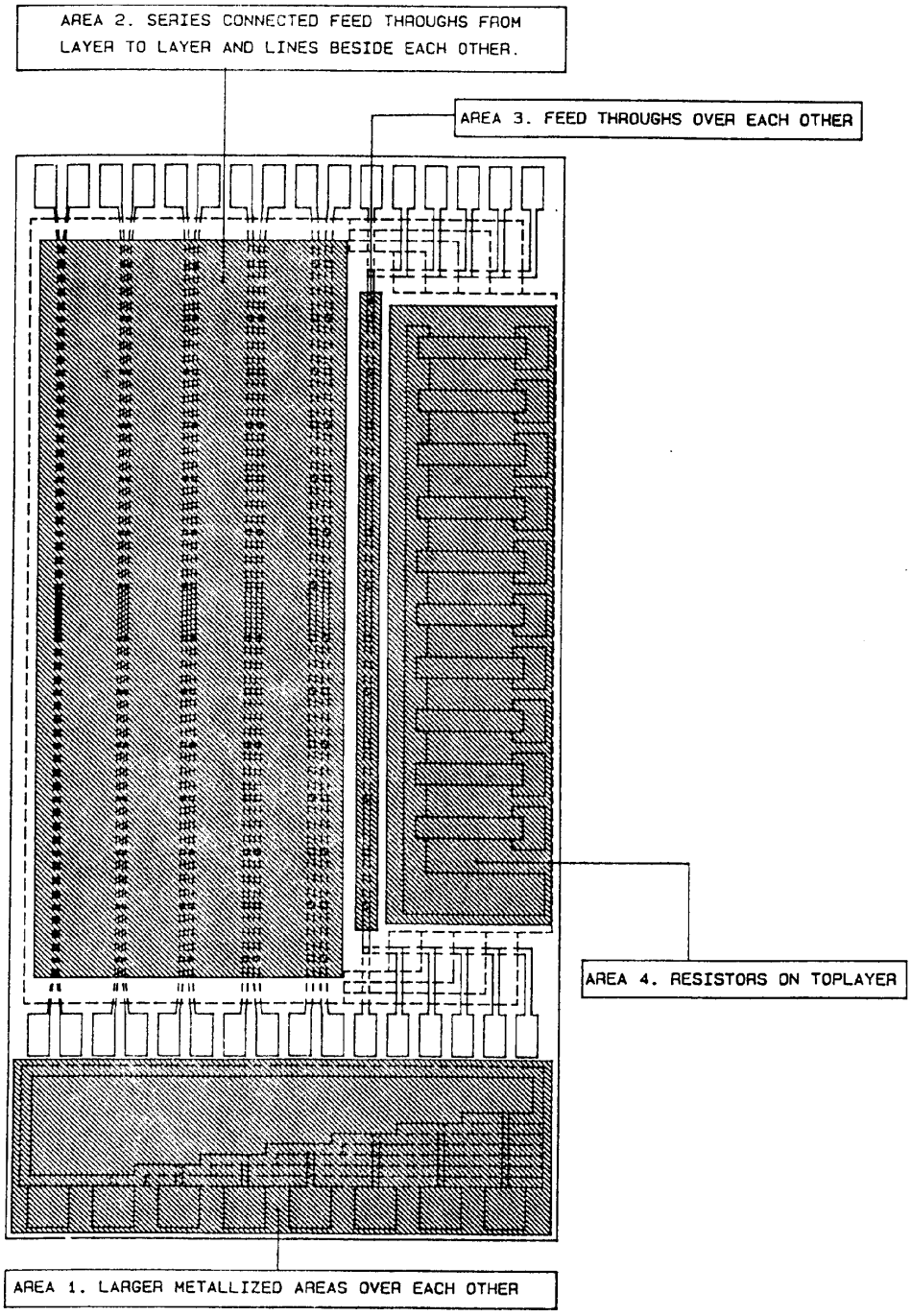
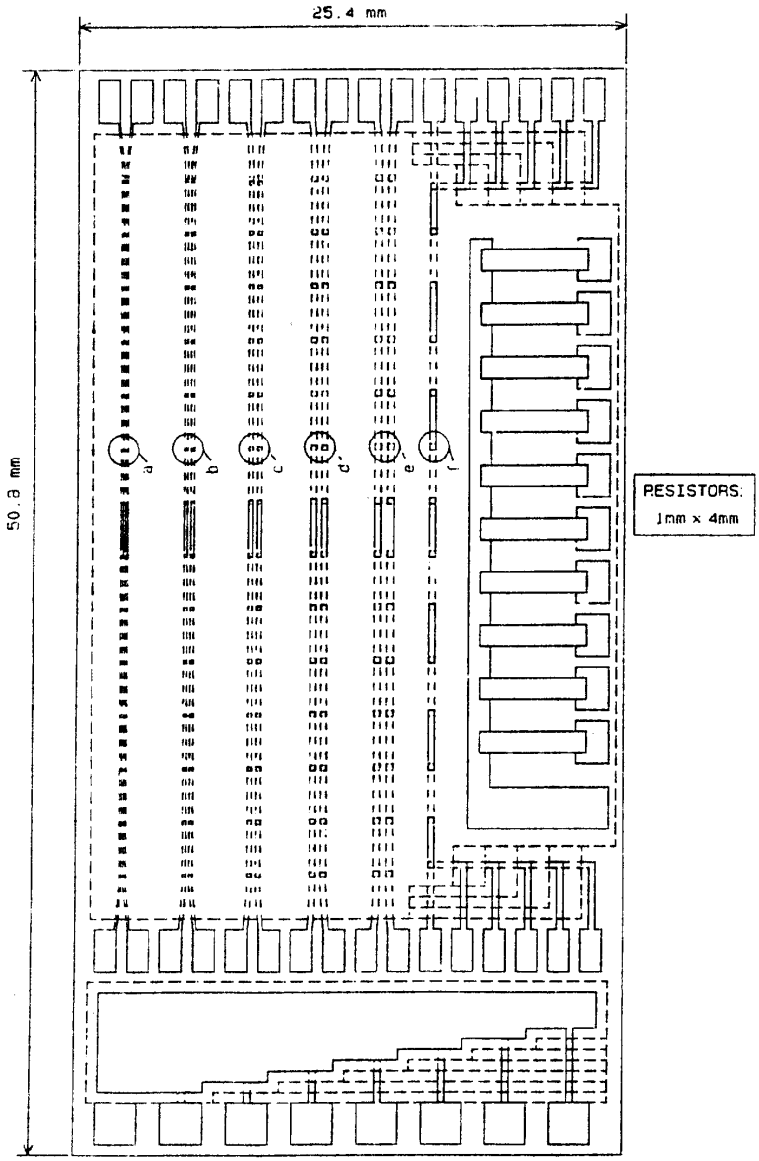


FIGURE 3 - DEFINITION OF TEST STRUCTURE B1 AREAS



	a	b	c	d	e	f	
LINE WIDTH	0.1	0.15	0.2	0.25	0.3	0.3	mm
LINE DISTANCE	0.1	0.15	0.2	0.25	0.3	-	mm

FIGURE 4 - LINE AND RESISTOR DIMENSIONS FOR TEST STRUCTURE B1

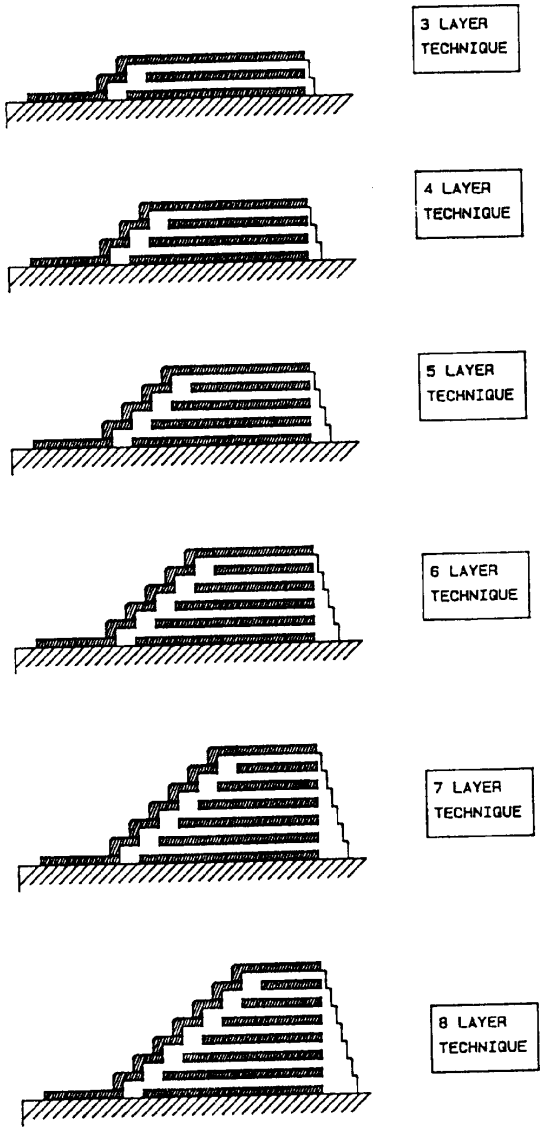


FIGURE 5 - DETAILS OF AREA 1 - METALLISED AREAS OF TEST STRUCTURE B1

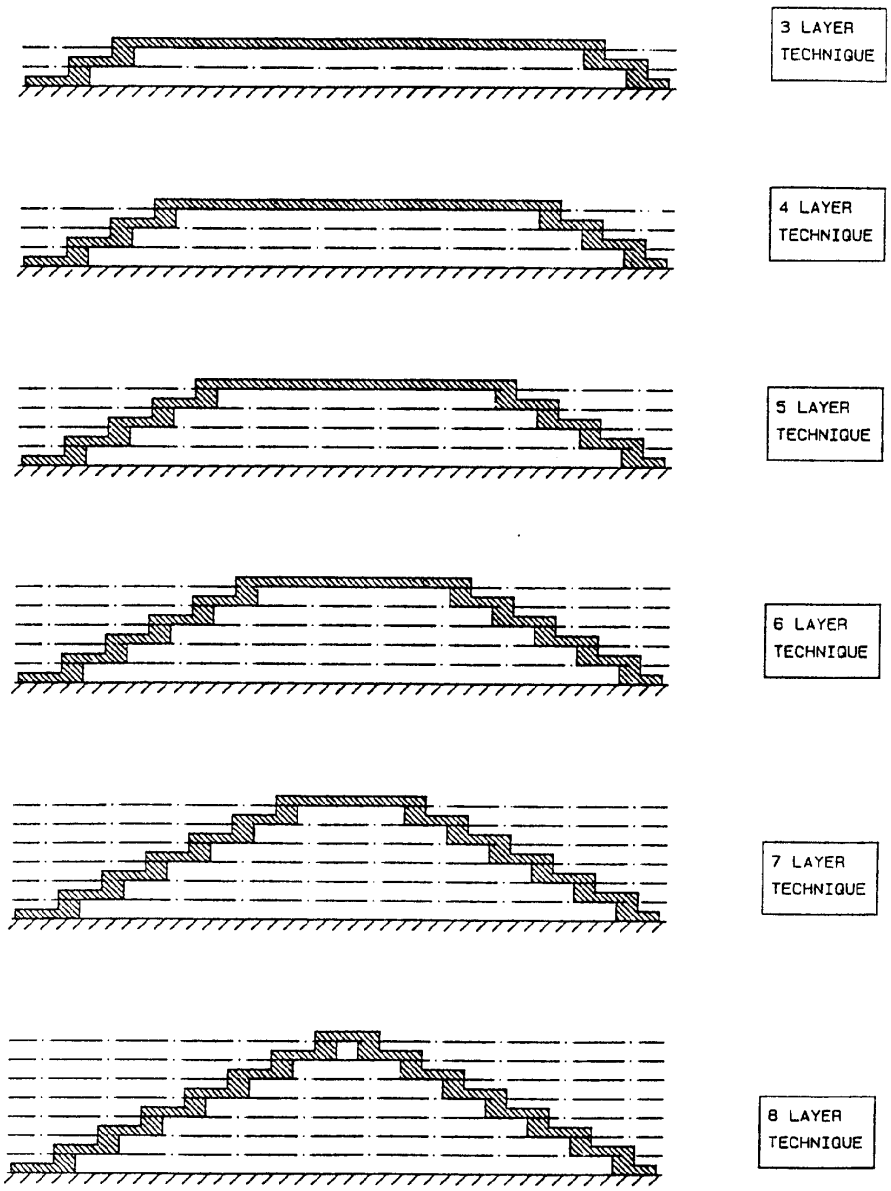


FIGURE 6 - DETAILS OF AREA 2 - SERIALLY CONNECTED FEED-THROUGHS OF TEST STRUCTURE B1

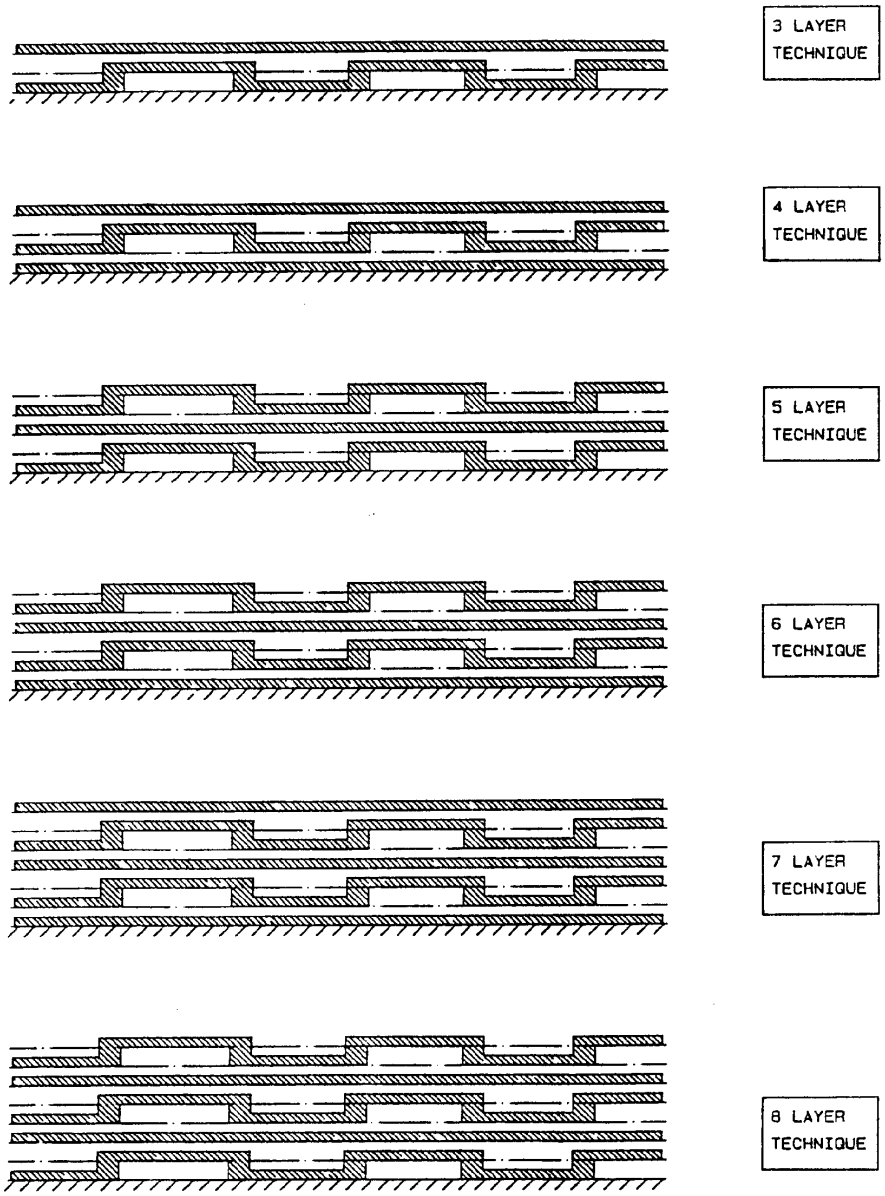


FIGURE 7 - DETAILS OF AREA 3 - FEED-THROUGHS OVER EACH OTHER - TEST STRUCTURE B1

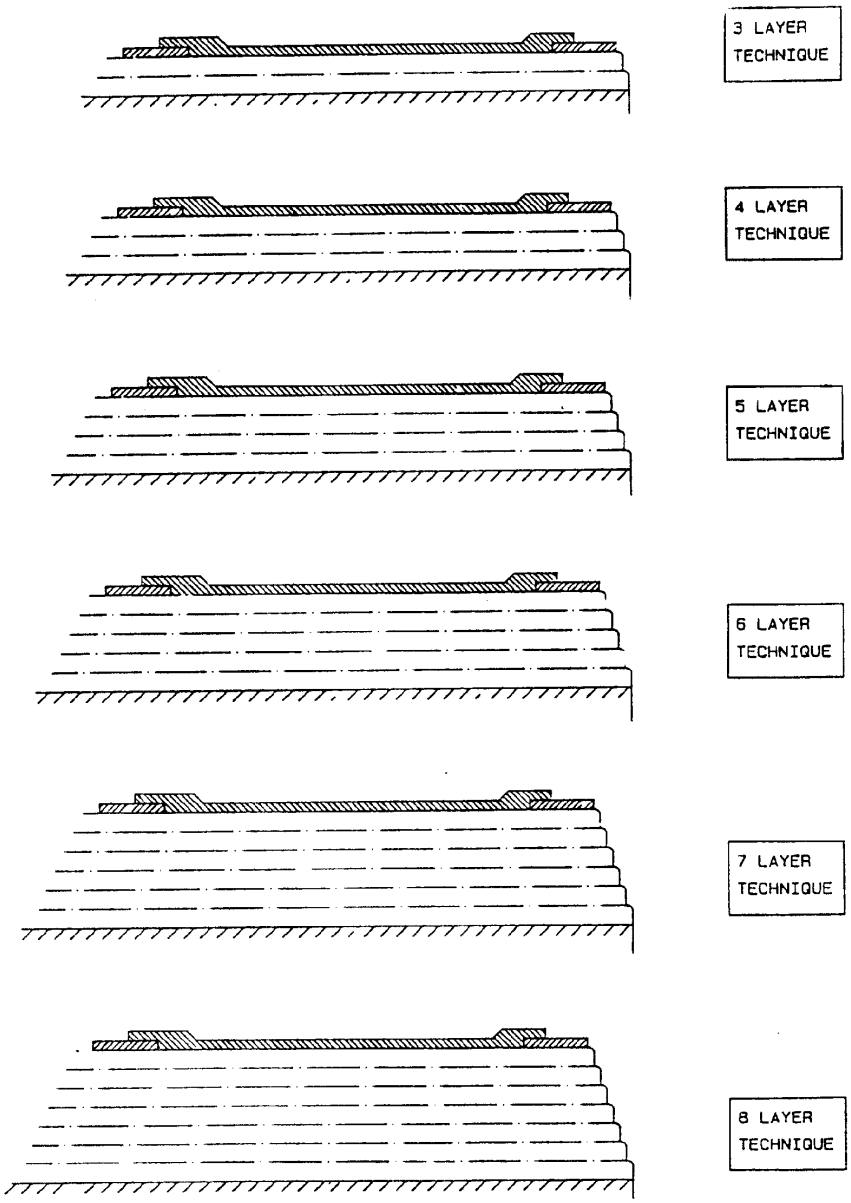


FIGURE 8 - DETAILS OF AREA 4 - RESISTORS ON TOP LAYER - TEST STRUCTURE B1

Endurance Testing

For evaluation of Test Structure B1, the following rules shall be applicable to Test 5, "Endurance Testing" specified in Table 8 and Para 3.2.6:

Thick Film Resistors

0.1 W, maximum 100 V d.c.
Load cycle: 90 minutes on, 30 minutes off.

Area 1 - Large Metallised Areas

100 V d.c. continuous over each insulation layer.

Area 2 - Serially Connected Feed-throughs

100 V d.c. continuous between each pair of lines.

Area 3 - Feed-throughs over each other

100 V d.c. continuous over each insulation layer.

b) Test Structure B2, covering Component Attachment

A generic lay-out of the pattern is given in Fig. 9.1.
The manufacturer shall design the lay-out applicable to his own technology. The following suggestions are to be considered as an example.

Substrate : 25.4 x 50.8 mm.

Components:

The components which can be attached to the thick-film network are usually of the following types:

- Active chips eutectically or epoxy-bonded directly to the substrate;
- Active chips as above, but attached to an open carrier (ceramic or molytab);
- Passive chips (capacitors or resistors) glued, soldered or wire-bonded to the substrate;
- Chip-carriers (leadless or leaded).

As a general rule, some components of both the smallest and largest size of each type shall be attached. If there is not enough space to accommodate all of the component types, they may be distributed over several test structures.

Figure 9.2 shows an example of a detailed lay-out of test pattern B2.

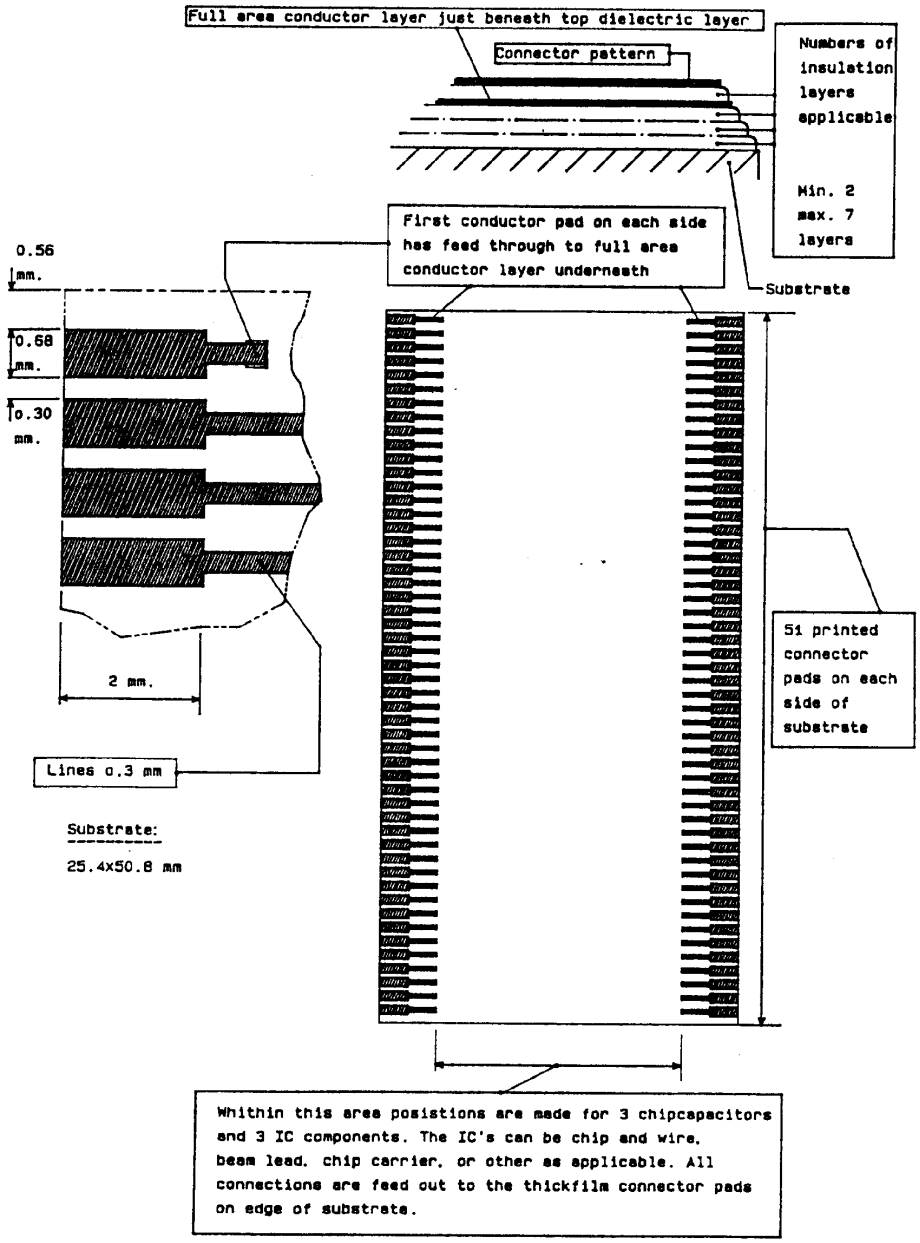


FIGURE 9-1 - TEST STRUCTURE B2 - MULTILAYER COMPONENT ATTACHMENT

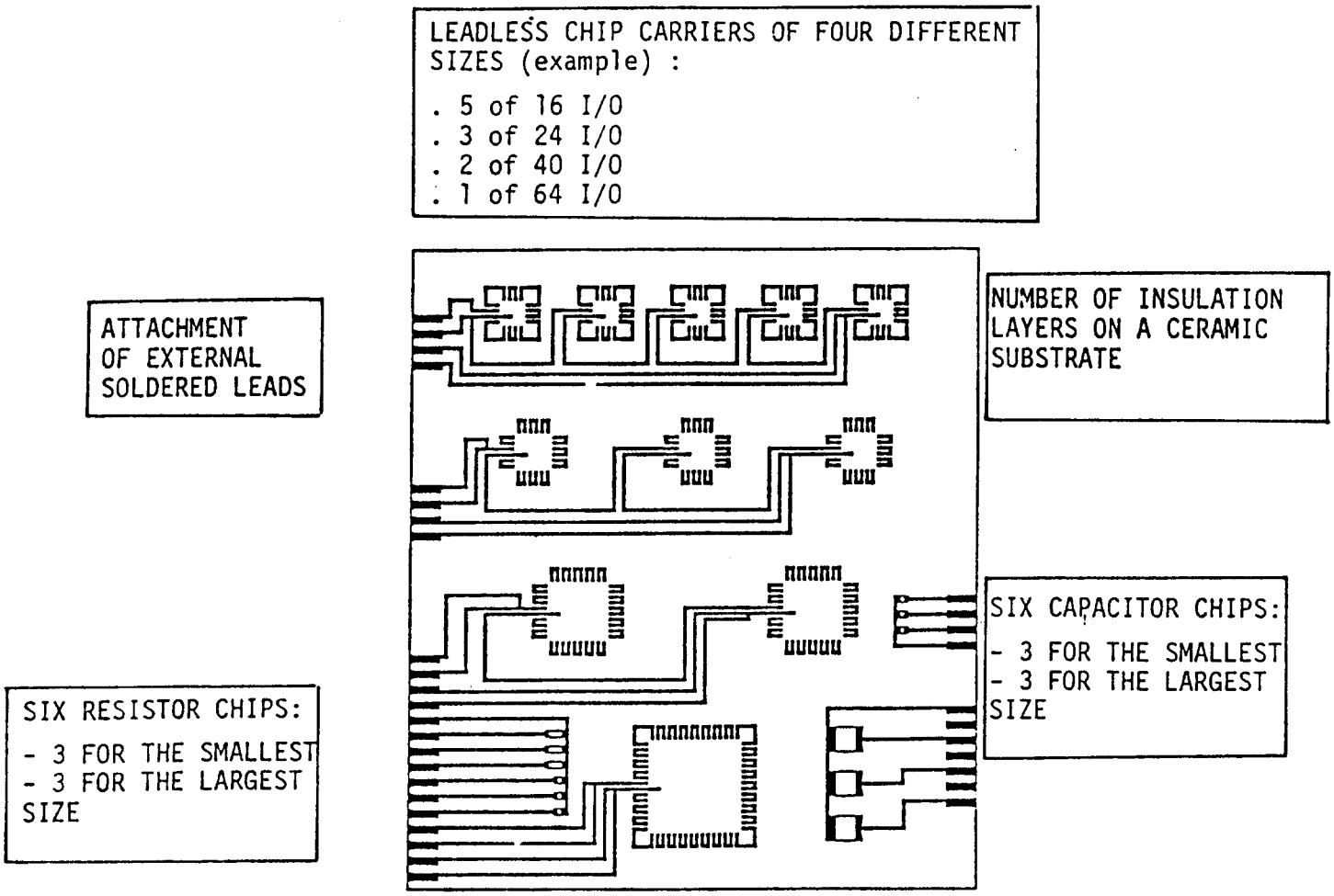


FIGURE 9-2 - TEST STRUCTURE B2 - EXAMPLE OF LAY-OUT

Printing Layers

The chosen number of dielectric layers shall be printed over the entire substrate. The pattern for capacitor and IC mounting shall be printed on top of these dielectric layers. Immediately underneath the top dielectric layer, there shall be a conductive layer to enable dielectric testing of the overlying component attachment pattern.

Packaging

Depending on the mounting or encapsulation method to be qualified, the test structure may be mounted on a baseplate, unmounted or encapsulated in a hermetically sealed package. If a hermetically sealed package is used, there shall be sufficient internal connections to permit the electrical testing of the attached components.

Rules for Endurance Testing

For evaluation of Test Structure B2, the following rules shall be applicable to Test 5, "Endurance Testing" specified in Table 8 and Para 3.2.6.

Top Insulation Layer

100 V d.c. continuous between top conductor layer with all terminals connected together and conductor layer printed immediately underneath.

Semiconductor Components and Chip Capacitors

No electrical load.

3.2.5.3 Test Structure C1 covering High-Power and High-Current Circuits

The relevant test pattern is shown in Figure 10 and details:

- A pair of high-power resistors, one having the lowest Ω/square value to be qualified and the other with a non-critical mean Ω/square value of 1 kΩ/square.
- A position for the mounting of a high-power semiconductor component and the applicable chip-carrier and connection system. The type with the highest power dissipation shall be used.
- A high-current conductor circuit consisting of a 8 x 12.5 mm conductor area with termination.

Packaging

For non-hermetic encapsulation, the substrate shown in Figure 10 shall be mounted on a metallic baseplate.

For hermetic encapsulation, the substrate together with the applicable internal connections and feed-throughs shall be mounted in the relevant package.

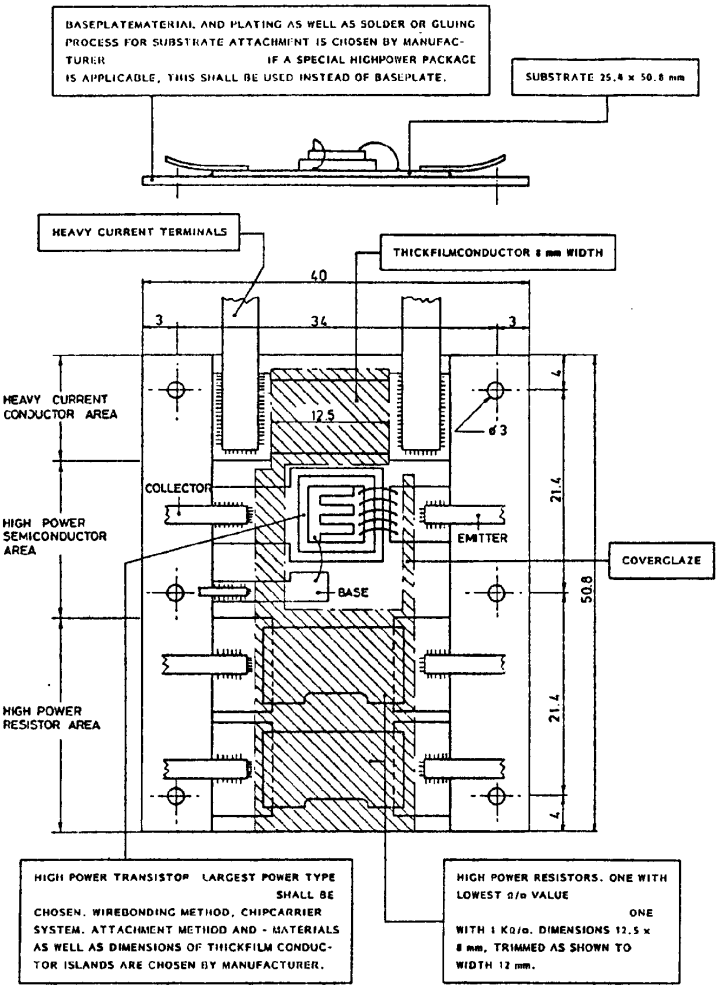


FIGURE 10 - TEST STRUCTURE C1 - HIGH-POWER AND HIGH-CURRENT CIRCUITS

Rules for Endurance Testing

For evaluation of Test Structure C1, the following rules shall be applicable to Test 5, "Endurance Testing" specified in Table 8 and Para 3.2.6.

Thick Film Resistors

Each resistor shall be loaded with 60 W d.c. or a.c.
Load cycle: 90 minutes on, 30 minutes off.

High Power Transistor

1.2 W d.c. per mm^2 area of silicon chip.

Heavy Current Circuit

16 A d.c. or a.c.

Mounting

The test structure shall be mounted on a water-cooled heat-sink having a surface temperature of +25°C.

3.2.5.4 Test Structure D1 covering High Voltage Circuits

The reason why Figure 11 shows the test pattern of a simple voltage divider system is that the main problems of a thick film high voltage circuit are created by resistors whose stability and accuracy are affected by temperature and voltage coefficient when used in precision voltage dividers.

Two versions of the circuit shall be made: one with a resistance paste giving resistor 'A' a value of 15 MΩ and the other with the highest Ω/square resistance paste. The voltage dividing ratio for trimming resistor 'B' shall be 100 : 1.

Package and Mounting Method

The substrate may be unmounted, mounted on a metal baseplate (see Figure 11) or mounted in a ceramic package with the applicable internal connection. If solder leads are used, they may be attached as shown.

Rules for Endurance Testing

For evaluation of Test Structure D1, the following rule shall be applicable to Test 5, "Endurance Testing" specified in Table 8, Para 3.2.6.

Thick Film Resistor - Voltage Divider

Load: 3 W, maximum 7500 V d.c.;
Load Cycle: 90 minutes on, 30 minutes off.

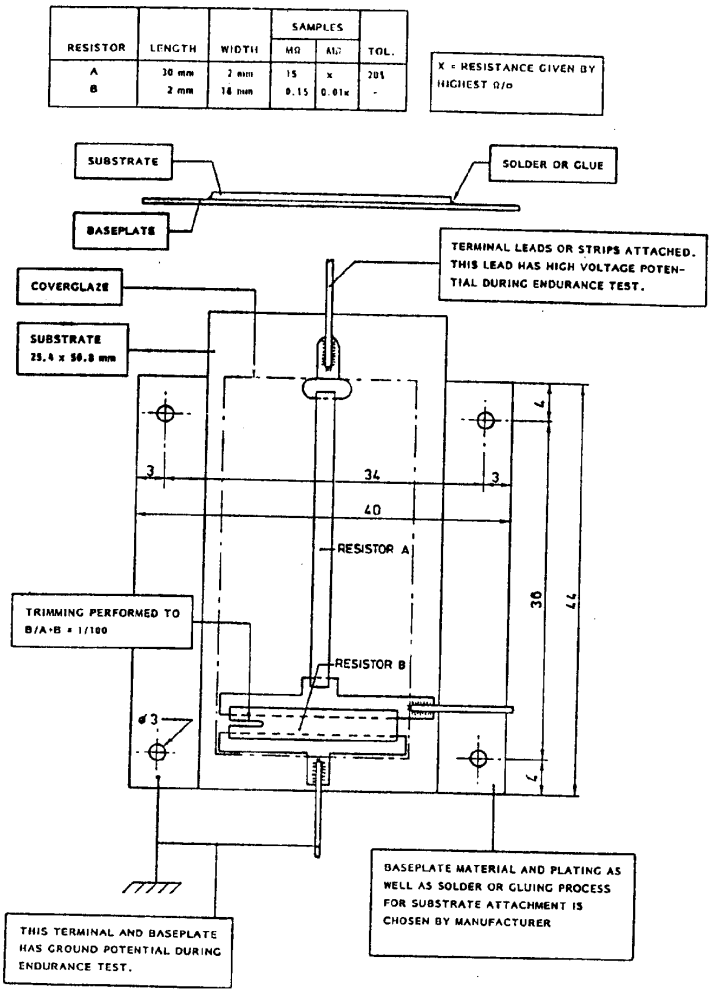


FIGURE 11 - TEST STRUCTURE D1 - HIGH-VOLTAGE HYBRID CIRCUITS

3.2.6 Evaluation Test Plans

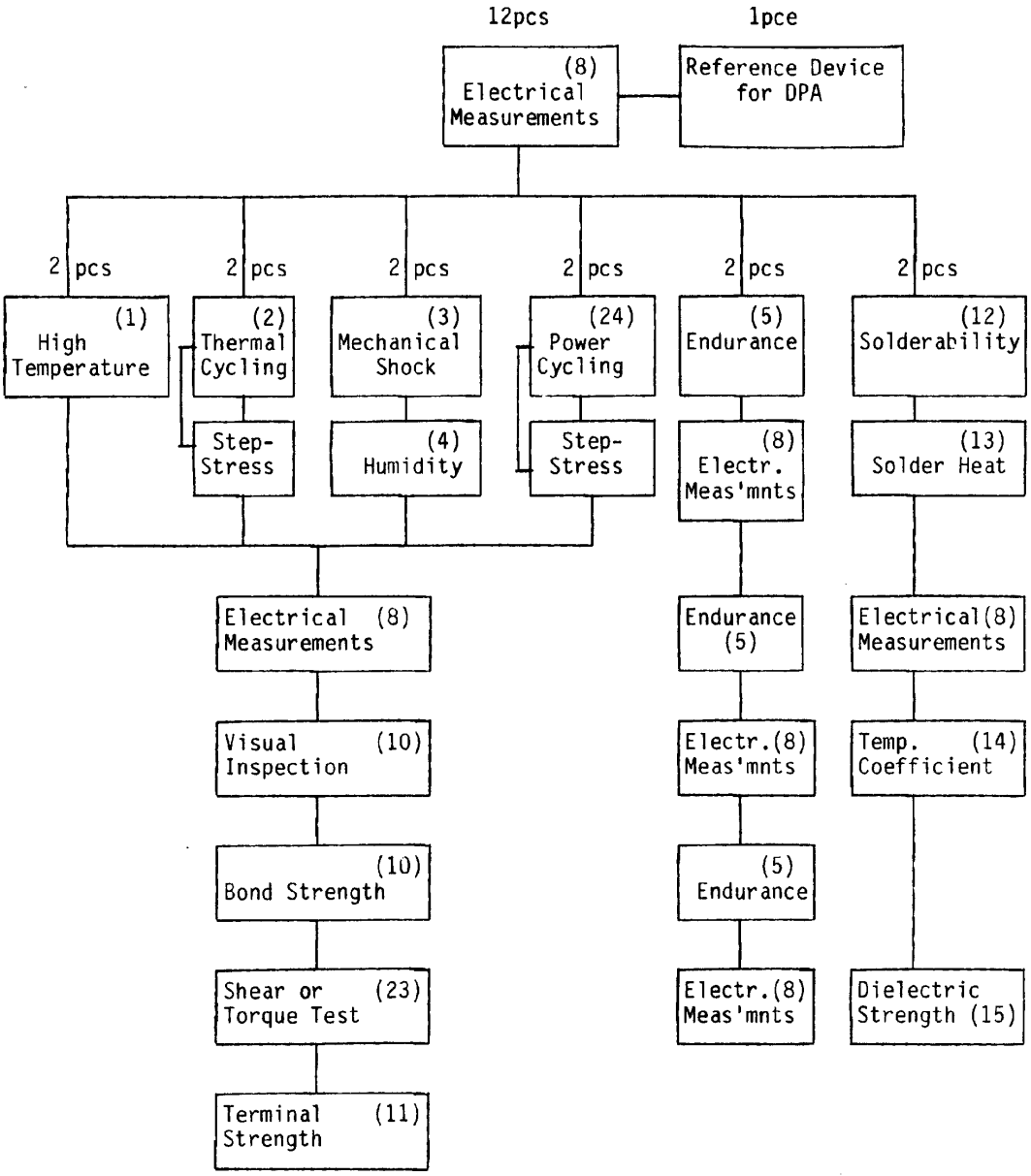
Testing, analysis of test results and presentation of the evaluation test programme shall be in accordance with the test plan and tables specified herein for each test structure. All structures and devices submitted to testing shall be clearly identified by serial numbers.

Upon completion of testing, all devices, test and inspection results, including a summary of all failure analysis results, shall be submitted to ESA. All measurements shall be recorded.

If verification of measuring equipment is required, the control devices shall serve for reference purposes.

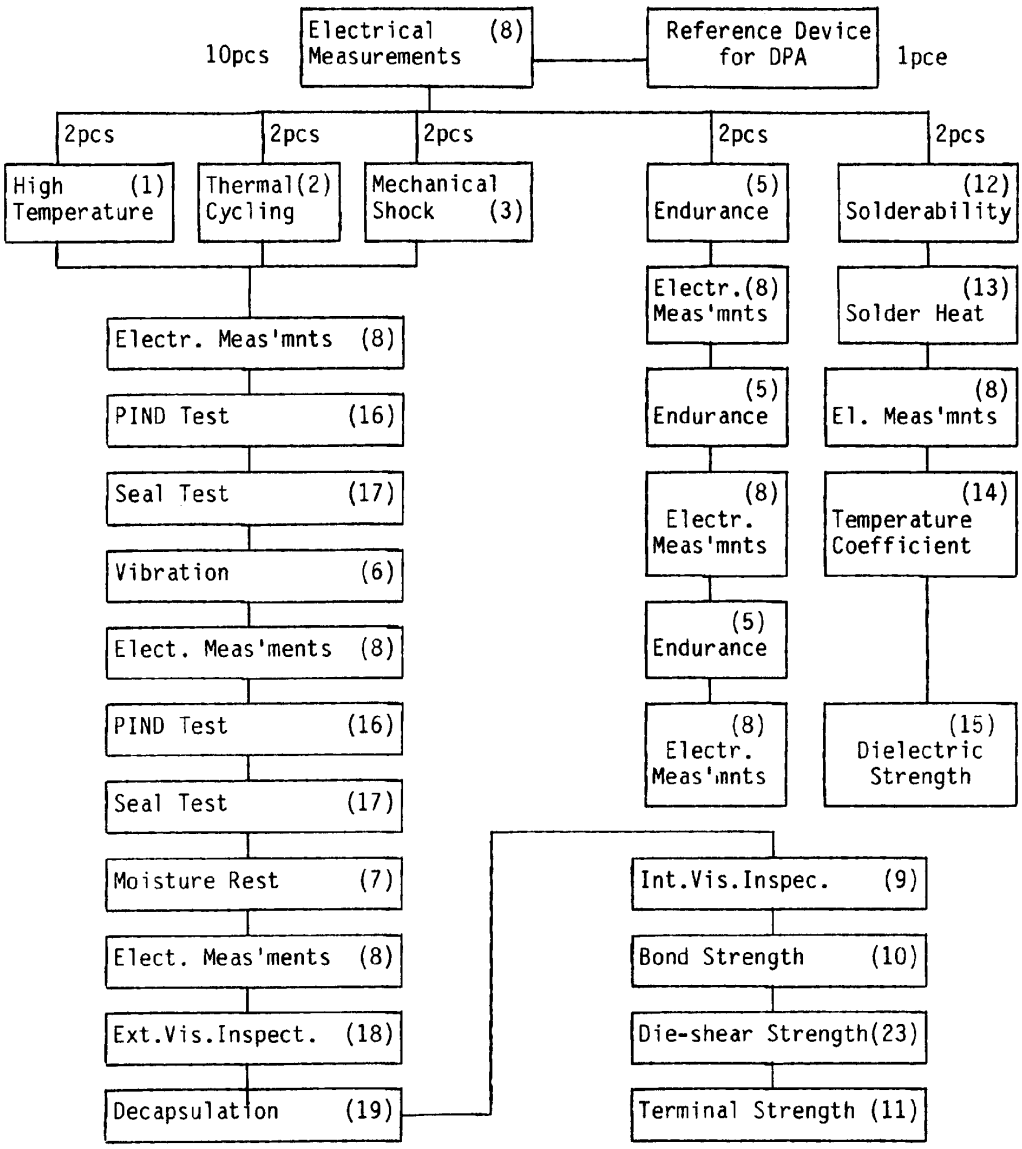
If termination and/or area identification numbers differ from those referenced in this specification, the manufacturer shall provide ESA with a cross-reference table.

The following test plans are applicable to the test structures specified in Table 7.



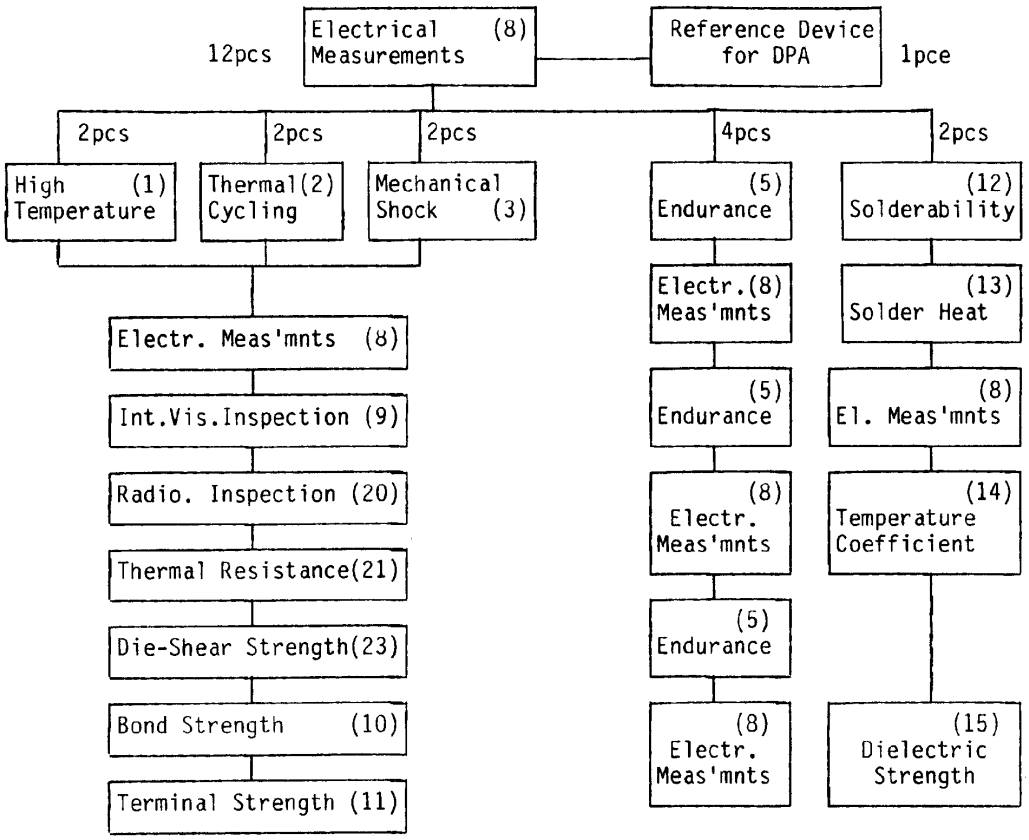
NOTE: Numbers in parentheses refer to test numbers of Table 8.

FIGURE 12 - TEST PLAN 1



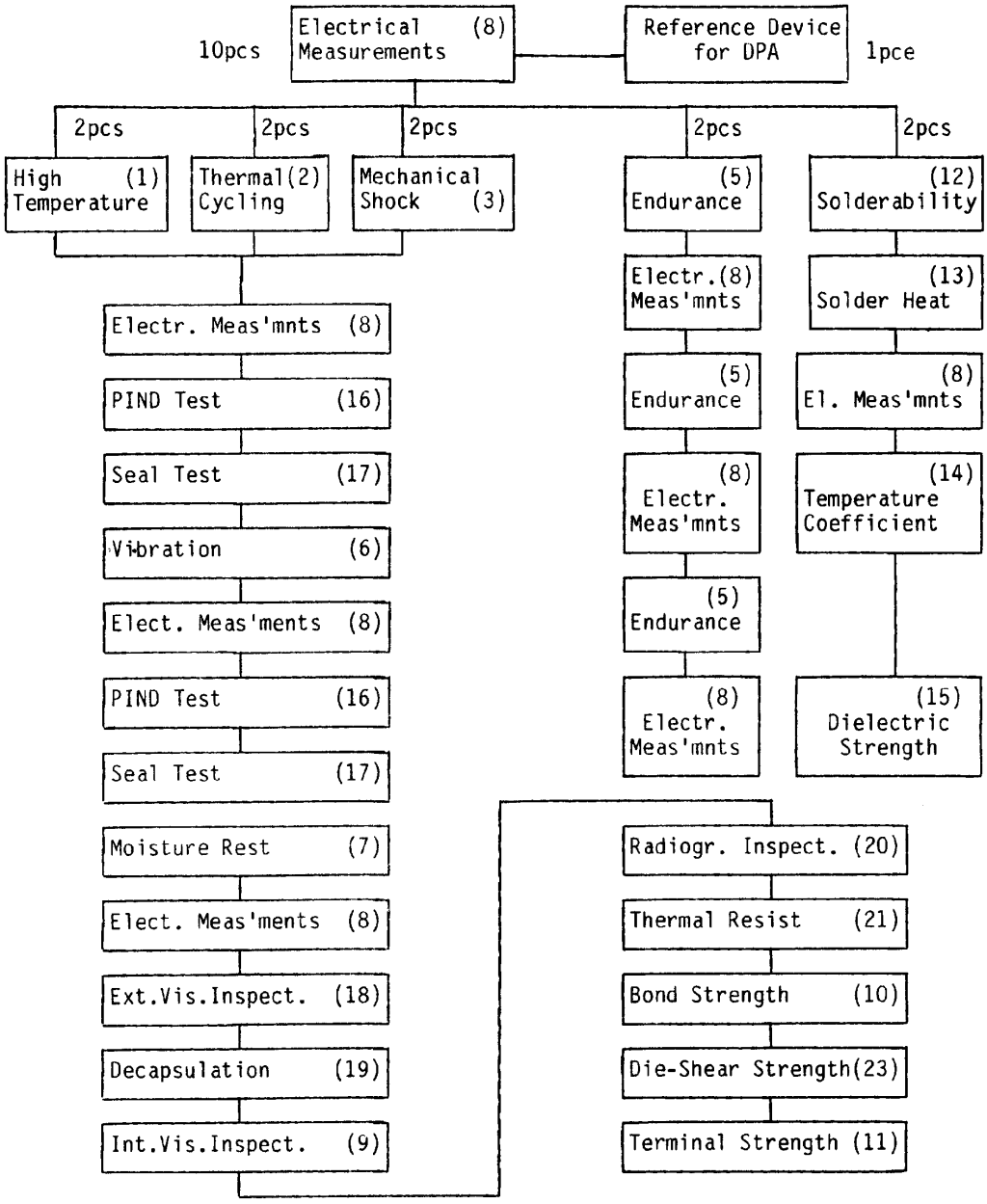
NOTE: Numbers in parentheses refer to test numbers in Table 8.

FIGURE 13 - TEST PLAN 2



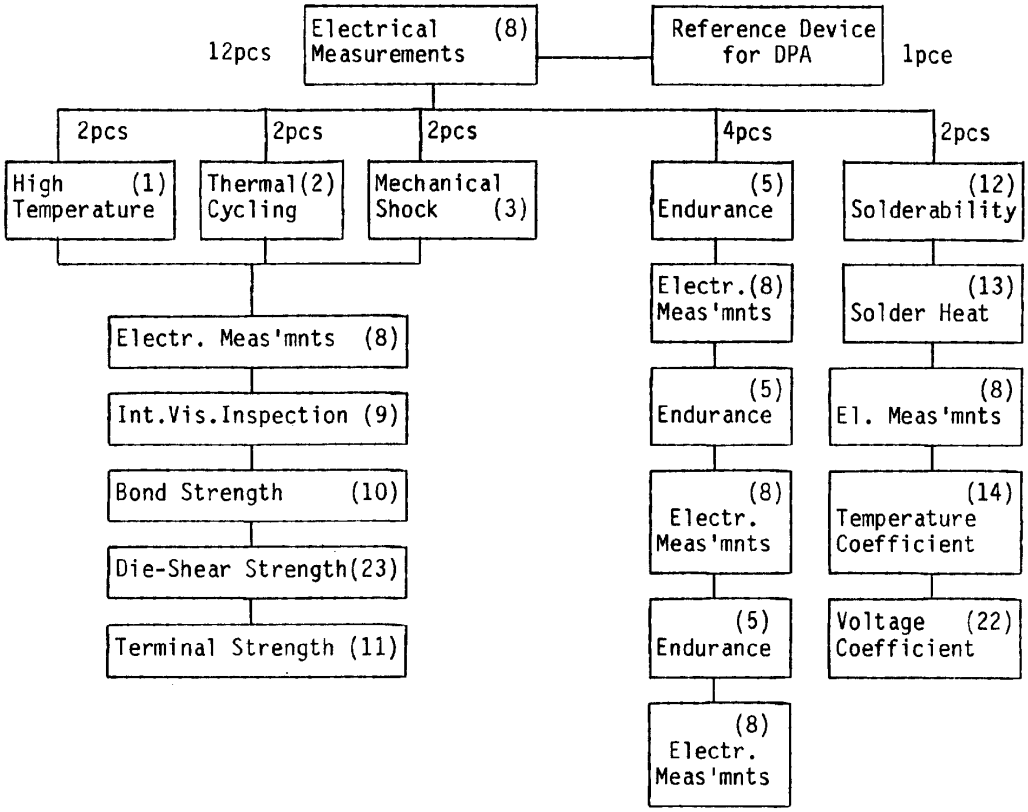
NOTE: Numbers in parentheses refer to test numbers of Table 8.

FIGURE 14 - TEST PLAN 3



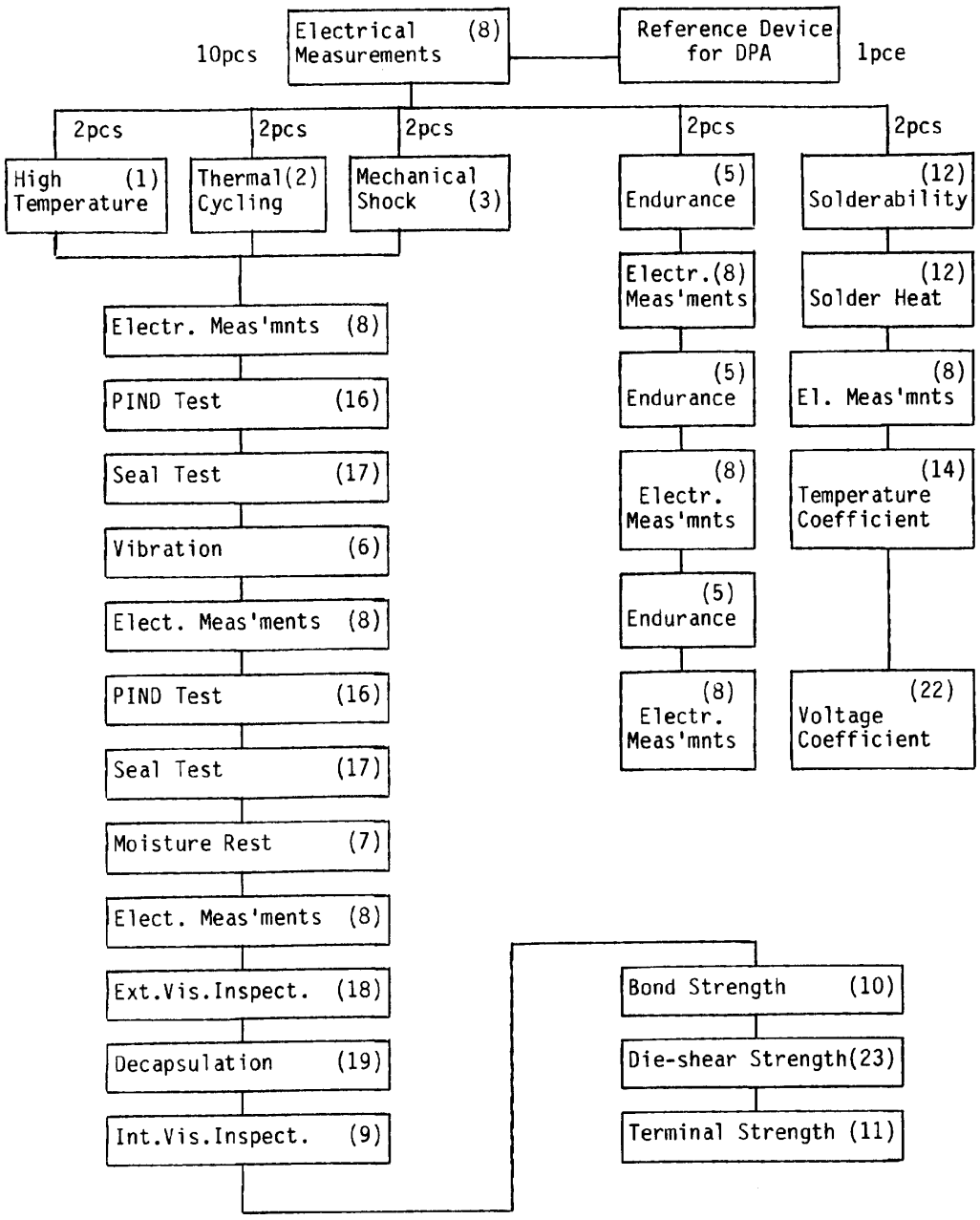
NOTE: Numbers in parentheses refer to test numbers of Table 8.

FIGURE 15 - TEST PLAN 4



NOTE: Numbers in parentheses refer to test numbers of Table 8.

FIGURE 16 - TEST PLAN 5



NOTE: Numbers in parentheses refer to test numbers of Table 8.

FIGURE 17 - TEST PLAN 6

3.2.7 Description of Tests

The test procedures pertinent to Test Plans 1 to 6 inclusive are listed in Table 8 together with reference to the applicable MIL specifications. The number of each test corresponds to that shown in the test plans.

Table 8 shall be used in conjunction with the supplementary test instructions specified for each of the individual test structures listed in Para 3.2.4.

TABLE 8 - TEST PROCEDURES

No.	Test	MIL-STD/Method		Test Conditions and Remarks
1	High Temperature Storage	883	1008	Condition 'B': +125° C; 2000 hours.
2	Thermal Cycling	883	1010	Condition 'B', 100 cycles per step up to 500 cycles or failure
3	Mechanical Shock	883	2002	Condition 'C', as per detail spec.
4	Humidity	202	103B	Duration 2000 hours, no voltage
5	Endurance	202	108A	Temperature: +125° C, Condition 'F' 2000 hours. Electrical load as specified in relevant test structure
6	Vibration	883	2007	Condition 'B', 50g. Test item shall be glued to the vibration fixture
7	Moisture Resistance	883	1004	10V d.c. between all terminals connected together and package; + on terminals
8	Electrical Measurements	202		
	- Resistance		303	Test accuracy: ± 0.05%. Printed Resistors
	- Capacitance		305	F = 1 MHz; Test accuracy on C = ± 0.1%. Registration of loss factor down to 0.001. Printed Capacitors and Chips
	- Insulation Resistance		302	Condition 'A', 100V. The test items are the same as specified for Test 15, "Dielectric Strength"
	- Semiconductor Components			Functional test. Electrical operational conditions shall be normal ones for component concerned. To be specified after joint agreement by ESA and manufacturer. For test points, see Para 3.4.3.1

TABLE 8 continued on next page.

TABLE 8 - TEST PROCEDURES (Continued)

No.	Test	MIL-STD/Method		Test Conditions and Remarks
9	Internal Visual Inspection	883	2017	Not applicable to hermetically sealed semiconductor components attached to substrate
10	Bond Strength	883	2011	Wire-bonds: Test Condition 'D'
11	Terminal Strength	883	2044	Flexible leads soldered to Thick Film Condition 'A'; Force = 30 x Q (Newton); Q = lead (mm^2) Flexible and Semi-flexible Leads in Packages As above. Rigid Feed-throughs in Packages D ≤ 1 mm: as above. Rigid Feed-throughs in Packages D > 1 mm: Condition 'C1'; Torque 1.5 N.cm
12	Solderability (Ext. termination)	202	208	Three terminals per test item
13	Soldering Heat (Ext. termination)	202	210	Condition 'B'. Three terminals per test item. Visual inspection by microscope (Magnification X4) to verify that terminals, glass seals, connection to thick film substrate or substrate itself are not damaged.
14	Temperature Coefficient (of printed resistors)	202	304	Maximum temperature: +125° C; Minimum " : -55° C
15	Dielectric Strength	202	301	Test Voltages Thick film pattern (all terminals connected together) to plate on reverse side of substrate, to baseplate or package: 200V d.c. Printed capacitors, cross-overs and between layers in multilayer system: 100V d.c.
16	Particle Impact Noise Detection (PIND)	883	2020	Condition A

TABLE 8 continued on next page.

TABLE 8 - TEST PROCEDURES (Continued)

No.	Test	MIL-STD/Method		Test Conditions and Remarks
17	Seal Test	883	1014	Step 1: Condition A1 or A2; Step 2: Packages with lids of 3 cm^2 and less: Condition C2; Packages with lids of 3 cm^2 and more: Condition C1
18	External Visual Inspection	883	2009	
19	Decapsulation	Lid shall be removed in such a way that interior of package is not contaminated		
20	Radiographic Inspection	883	2012	
21	Thermal Resistance	883	1012	Test Structure C1 only.. The thermal resistances of the - Thick Film Resistors, - Semiconductor Chips, - High Current Conductor are to be determined. The temperatures on internal connection strips and package feed-throughs shall be measured
22	Voltage Coefficient	202	309	During endurance testing, test voltage corresponds to load voltage (see Test 5)
23	Die-shear Strength	883	2019	Shall be performed also on chip capacitors, chip resistors and leadless chip carriers attached to the substrate. Alternatively, torque test may be performed on leadless chip carriers
24	Power Cycling	-	-	All components to be powered at nominal power dissipation level. Power shall be switched on and off 500 times (cycles). Lapse time for each cycle shall be 3x time constant. Power shall be increased in steps up to failure.

3.2.8 Detail Specifications of Test Structures

The manufacturer shall write a detail specification of each test structure to be evaluated. Each specification shall contain tables of the detailed electrical measurements to be performed before and after exposure to environmental tests. The following details shall be stated:

a) **Line-printing quality**

Statement of minimum line-width and line-distance.

b) **Thick Film Resistors**

Manufacturing tolerance	:	± 20% (untrimmed), ± 1% (trimmed);
Maximum change during test	:	± 2%;
Maximum temperature coefficient calculated for any range between two test temperatures	:	As specified by the manufacturer;
Maximum voltage coefficient	:	As specified by the manufacturer;
Visual Inspection	:	As per MIL-STD-883.

c) **Capacitors, Thick Film, Printed**

Manufacturing tolerance	:	± 20%;
Maximum change during test	:	± 2%;
Maximum change of loss factor during test	:	1.5 x initial value;
Insulation resistance	:	$10^{10}\Omega$ minimum;
Dielectric strength	:	As per MIL-STD-202;
Visual Inspection	:	As per MIL-STD-883.

d) Capacitors, Attached Chips

Maximum loss factor	:	As specified by chip manufacturer;
Maximum change of loss factor during test	:	1.5 x initial value;
Insulation resistance	:	10^{10} minimum;
Dielectric strength	:	As per MIL-STD-202;
Bond strength	:	As per MIL-STD-883;
Visual inspection	:	As per MIL-STD-883.

e) Printed Cross-overs and Multilayer Systems

Insulation resistance	:	$10^{10}\Omega$ minimum;
Dielectric strength	:	As per MIL-STD-202;
Visual inspection	:	As per MIL-STD-883.

f) Semiconductors, Attached

Electrical functional test	:	Test limit to be agreed jointly by manufacturer and ESA;
Bond strength	:	As per MIL-STD-883;
Visual inspection	:	As per MIL-STD-883.

g) Wire Cross-overs, Internal Connections

Bond strength	:	As per MIL-STD-883;
Visual inspection	:	- ditto -

h) External Connections and Leads

Terminal strength	:	- ditto -
Visual inspection	:	- ditto -
Solderability	:	As per MIL-STD-202;
Soldering heat	:	- ditto -

i) **Assembly and Package**

Internal visual inspection	:	As per MIL-STD-883
External visual inspection	:	- ditto -
PIND test	:	- ditto -
Seal test	:	- ditto -
Radiographic inspection	:	- ditto -

j) **Thermal Characteristics of High Power Structures**

Thermal resistance to heat sink of:

Each thick film resistor	:	Maximum 1.5° C x cm^2/W (*);
Semiconductor chip	:	Maximum 0.75° C x cm^2/W (*); Maximum 85° C for soft soldered connections.
Temperature of connection leads		Maximum 100° C for welded or wire-bonded connections.

(*) cm^2 area of thick film resistor or semiconductor chip.

k) **Structures with Base-plate**

Visual inspection	:	As per MIL-STD-883;
Radiographic inspection (power structures)	:	Area of void(s) under dissipative source shall not be more than 25% of the area of that source. Total void area (sum of all voids at substrate/base-plate interface) shall not exceed 25% of substrate area.
Insulation resistance	:	Minimum $10^{10}\ \Omega$.

3.2.9 Failure Analysis

All failed items shall be subjected to failure analysis. The applied procedure shall enable determination of the cause of failure, failure mode and any corrective action required. A detailed test report of all failed items shall be submitted to ESA.

3.3 EVALUATION REPORT

The manufacturer shall produce an Evaluation Report in compliance with this specification and signed on behalf of the company.

3.3.1 Analysis of Results

At the end of the Evaluation Phase, ESA will analyse the results of:

- Line survey,
- Evaluation testing.

Based on the outcome of this review, ESA will decide whether the manufacturer may proceed to the next phase of the programme or whether any corrective actions are required.

3.3.2 Corrective Actions

ESA may recommend certain modifications in the manufacturer's organisation, the production line and/or processes. If the manufacturer wishes to proceed to the next phase, he shall implement such modifications.

If major changes are deemed necessary, ESA may require repetition of certain evaluation tests and/or re-evaluation of test results.

3.3.3 Process Identification Document (PID)

The manufacturer shall establish a PID, specifying the agreed procedures for manufacturing control. Details of the contents of the PID are given in Para 4.2.

3.4 COMPLETION OF EVALUATION PHASE

Upon satisfactory completion of the Evaluation Phase, ESA will agree the definition of the manufacturer's capabilities and give its consent to proceed to capability approval testing.

4. CAPABILITY APPROVAL TESTING PHASE

4.1 GENERAL

The Capability Approval Testing Phase shall cover all tests approved by ESA upon completion of the Evalution Phase and consist of:

- the freezing of the processes, process and inspection documents, and materials defined in the Process Identification Document (PID) and
- the manufacture and testing of either test structures or actual circuit types.

4.2 PROCESS IDENTIFICATION DOCUMENT (PID)

Prior to the manufacture of the test structures to be subjected to testing, the manufacturer shall prepare the PID and agree its contents with ESA. The PID shall be divided into sections according to the following guidelines referencing each process to be applied:

Section 1

- Cover page, showing title of PID, issue number and date, and - if applicable - revision letter and date;
- Revision list, showing revised pages and dates of revision,
- List of contents, showing PID sections.

Section 2

Flow-chart of manufacture, assembly and testing with reference to the cable specifications (a specimen flow-chart is shown in Figure 18).

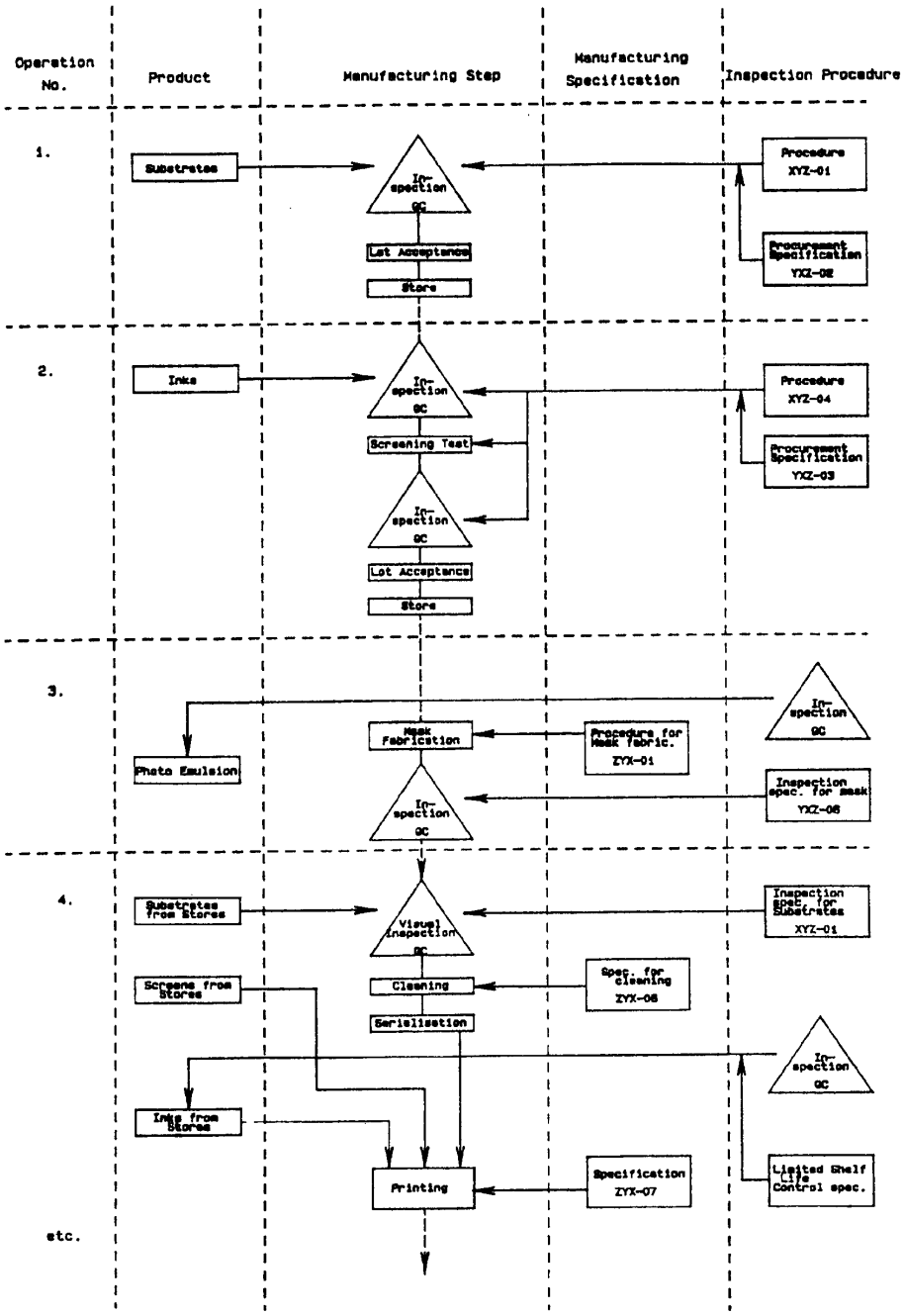


FIGURE 18 - EXAMPLE OF MANUFACTURING FLOW CHART

Section 3

List of specifications with titles, issue/revision numbers and dates referenced in the flow-chart, and used for the manufacture and control of the devices.

Section 4

Organisation of the company, including organigrams of:

4.1 Management,
4.2 Production department,
4.3 Quality department.

Section 5

Processing of hi-rel orders:

5.1 In-house processing flow-chart of hi-rel orders, showing the extent to which each department (Design Engineering, Reliability, Product Assurance, Production, Quality Control, etc.) is responsible for the execution of external orders for hybrid circuits.
5.2 Procurement options, viz. variants and testing levels of qualified hybrid microcircuits which the manufacturer can offer.
5.3 Specimen of a hi-rel traveller.
5.4 Points for inspection by orderer.

Section 6

List of subtechniques, materials and rework:

6.1 All subtechniques and associated test structures used shall be listed. This section shall include a colour photograph of the test structure(s) to be tested.

6.2 All materials, such as substrates, inks, epoxies (with infrared spectrum), wires, packages, etc., shall be listed together with the manufacturer's name, incoming inspection specification and, where applicable, the validation procedure.

6.3 Provisions for rework shall detail how, when, the number of times and according to what procedure, rework is permitted.

Section 7

Manufacturing line lay-out:

7.1 Overall line lay-out,

7.2 Details of testing area,

7.3 Dust, humidity and temperature control of the various areas.

Section 8

Equipment list.

Section 9

- List of failure analysis equipment.
- Standard failure analysis procedure.

Section 10

Records of lots processed according to the subject PID, including number(s) and type(s) of circuits, lot acceptance results and applicable qualification reports. This section shall be annually updated.

The information contained in this section shall be arranged as exemplified in Table 9 and, as a minimum, include the items listed therein.

The established PID shall be called up automatically in any documentation applicable to deliveries according to this specification or ESA Procurement Specification PSS-01-608. Any deviations from the PID shall be subject to prior ESA approval.

TABLE 9 - EXAMPLE OF PID - SECTION 10 INFORMATION

Programme or Project	No.of hybrids produced	Screening Level	Description of Circuit	Spec. No.	Lot No.	Lot Qual. Report
EXOSAT	20	B	Control Circuit	XYZ-123	8230	ABC-456

The complete PID, comprising all called-up specifications, shall be kept by the manufacturer at the production plant; it shall be made available to ESA or its designated representative for review.

A condensed PID, comprising all basic information, e.g. flow-charts, lists of specifications, materials and processes, but complemented by copies of only the most important specifications, shall be kept by ESA and treated as proprietary information.

The PID shall be made available to the Purchaser for inspection.
The production flow-chart shall always be made available to the Purchaser upon request.

Travel-logs shall include all processing details, dates and yields of process steps and any useful comments. They shall be signed or stamped on behalf of the manufacturer's Quality Assurance department in respect of those operations that are listed as functions of that department. The manufacturer shall keep the travel-logs for a minimum period of three years and, upon request, make them available to ESA, its designated representative, or the Purchaser.

4.3 DETAIL SPECIFICATIONS

Before testing is started, all detail specifications of test structures shall be prepared by the manufacturer and submitted to ESA for approval. They shall be written according to Annex 'B' of ESA PSS-01-608.

4.4 MANUFACTURE OF TEST STRUCTURES

Lot manufacture shall be in accordance with the approved PID and all parts thereof shall be selected and screened to level B as per Specification ESA PSS-01-608.

ESA reserves the right to participate in precap visual inspection.

4.5 ADDED-ON COMPONENTS

See Specification ESA PSS-01-608.

4.6 REWORK

Some of the hybrids submitted for testing shall have been reworked according to the methods described in the PID.

General rules for rework are as specified in MIL-M-38510 for Class 'S' devices.

4.7 LOT PRODUCTION REPORTS

The manufacturer shall submit to ESA reports of:

- screening (including burn-in parameter drift values),
- final acceptance test,
- failure analysis of parts failed during screening,

- in/out figures relevant to the following inspections and tests:

  - visual inspection and final test of thick film network,
  - pre-seal acceptance test,
  - screening,
  - final acceptance test.

The in/out figures shall be recorded in terms of the number of parts submitted for a specific test, or group of tests, and the number of rejects. Failure mode data shall be included.

4.8 TEST PLAN

The manufacturer shall prepare and submit to ESA for approval a test plan, including a specification of each test structure and a time schedule for production and tests. The time schedule shall show the dates envisaged for performance of the following milestone operations:

- start of manufacture,
- start of pre-seal acceptance test,
- start of screening and final test,
- start of mechanical, environmental and endurance tests,
- completion of mechanical, environmental and endurance tests.

The manufacturer shall notify ESA, or its delegated representative, as soon as each of these operations has been completed.

All documents specified herein for review by ESA shall be submitted at least 22 working days before either the due review date or the date on which the manufacturer intends to proceed to the next action in the sequence of operations.

4.9 CAPABILITY APPROVAL TESTING

4.9.1 Hermetic Thick Film Hybrid Microcircuits

Testing shall be performed in accordance with the test plan shown in Figure 19 for a general-purpose low-power hybrid microcircuit, encapsulated in a package and the requirements defined in the following subparagraphs.

The total number of test structures shall depend on the number of structures/types to be tested. It may be necessary to test more than one type of structure. If so, the number of structures specified in Table 10 shall be applicable. The lay-out of the test structure(s) may be identical to that of any structure specified for the Evaluation Phase or that of a new structure.

Satisfactory test results of reworked test structures shall automatally imply the acceptance of non-reworked test structures.

In case of several types of test structure, they shall be distributed over the various subgroups as shown in Table 10.

TABLE 10 - NUMBER OF TEST STRUCTURES FOR CAPABILITY APPROVAL
(Hermetic Hybrids)

No. of Test Structure Types	Number of types required per subgroup						Total No. per Type
	I	II	III	IV	V	VI	
1	6	6	3	2	10	6	33
2	3	3	2	1	6	3	18
3	2	2	1	1	4	2	12

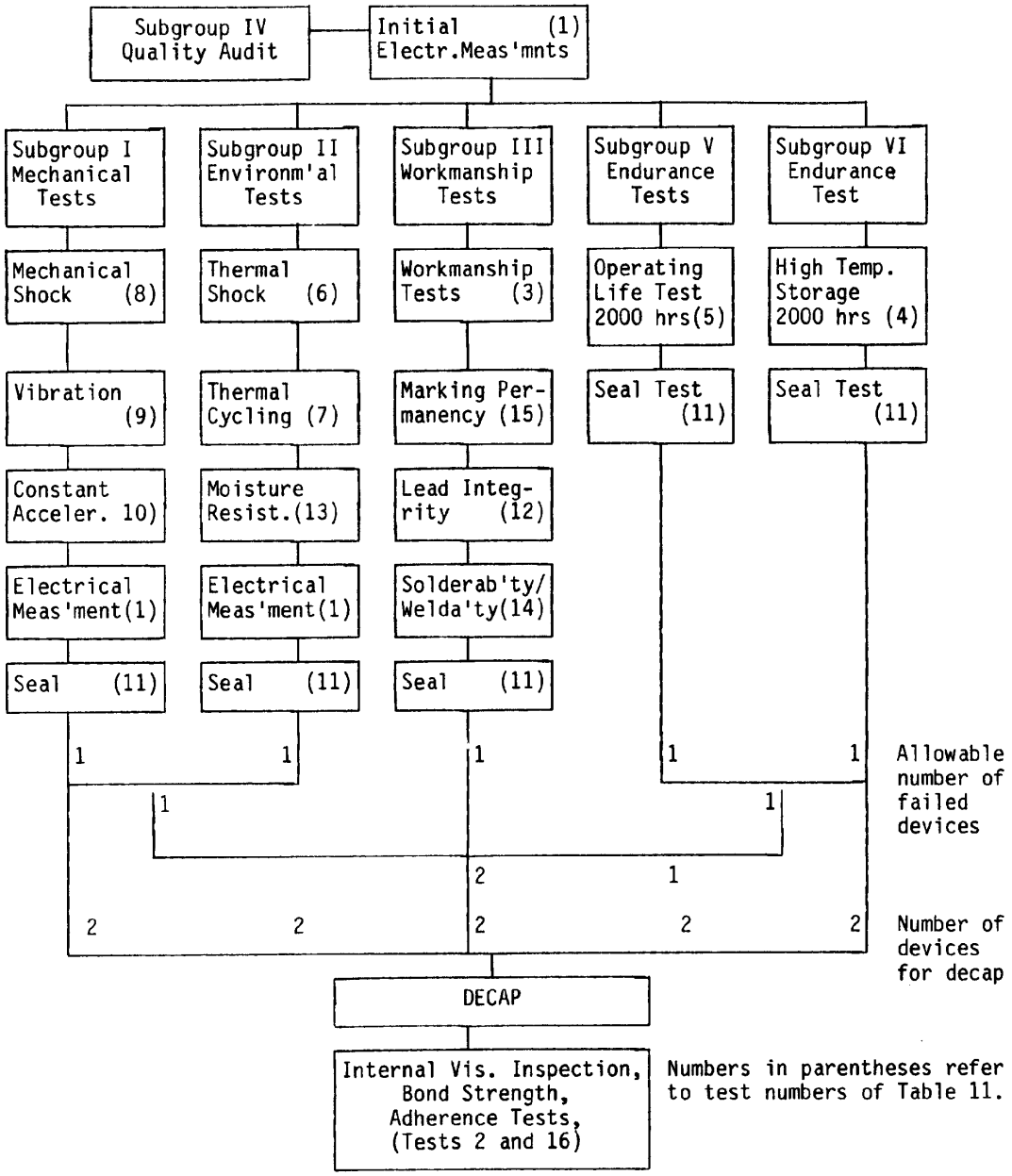


FIGURE 19 - TEST PLAN FOR HERMETIC HYBRIDS

4.9.1.1. Subgroup III, Workmanship

Workmanship shall be assessed as follows:

- Radiographic inspection,
- External visual inspection (including marking),
- Physical dimensions and weight,
- Internal water vapour content.

4.9.1.1.1 Radiographic Inspection

This inspection shall be performed in accordance with MIL-STD-883, Method 2012.

4.9.1.1.2 External Visual Inspection (including Marking)

This inspection shall be performed according to MIL-STD-883, Method 2009. The marking shall be inspected to ascertain its conformance to the requirements of the applicable test structure detail specification. It shall be legible and unambiguous. Any misalignment of the highest and lowest letters in a row shall not exceed 70% of the letter size. The overlapping of the lowest letters of one row and the highest letters of the next row shall constitute a failure.

4.9.1.1.3 Physical dimensions and Weight

All physical dimensions specified in the applicable detail specification shall be measured. Any nonconforming part shall be considered as a failure and contribute towards qualification failure. Two or more nonconforming dimensions of one part shall count as one failure.

All parts shall be weighed and the average weight per part recorded.

4.9.1.1.4 Internal Water Vapour Content

According to MIL-STD-883C, Method 1018.2, on 1 (one) package.

4.9.1.2 Subgroup IV, Quality Audit

The devices of this subgroup together with the results of the initial electrical test shall be sent to ESA for construction analysis as follows:

The devices of this group will be subjected to the inspections and operations defined in the following subparagraphs. A record will be made of each separate step and all records will be compiled and summarized in one report together with the analysis results.

a) **Decap**

The parts will be decapped or opened without damage to the functional elements. Any inspection of a decapped device will take place in a controlled atmosphere.

b) **Description**

Each part type will be described fully and photographed in such a way that the interior of the package and functional elements are highlighted. Descriptions will include measurement data of physical dimensions and relative location of added parts.

c) **Internal Visual Inspection**

The parts will be inspected for conformity to the applicable requirements of MIL-STD-883, Method 2017 and Condition 'A' of Method 2010).

Any visual anomalies will be microphotographed and the presence of any foreign matter will be recorded.

The parts will be inspected by a Scanning Electron Microscope (SEM) to verify that bonds, joints, trimming paths, metallisation steps, etc. meet the specified requirements. Each of these items will also be photographed.

d) **Bond Strength/Adherence Group**

The control devices will be submitted to the following tests of Table 11:

- Bond strength (Test 16a),
- Chip adherence (Test 16b),
- Substrate Adherence (Test 16c).

All test results, including failure categories will be recorded.

e) **Any Other Construction Analysis Tests**

For example: seal test, PIND test, water vapour content, etc.

TABLE 11 - TEST METHODS FOR HERMETIC HYBRIDS

No.	Test	MIL-STD-883, Method	Conditions and/or Remarks
1	Electrical Measurements	Electrical measurements of all parameters listed in the detail specification shall be performed in accordance with the test methods and conditions specified in that specification. All results shall be recorded and all samples allocated to testing shall be submitted to these electrical tests prior to the start of testing. There shall be no catastrophic electrical failures at this stage. Any such failures shall invalidate the approval. Any devices exhibiting electrical out-of-tolerance parameters shall be replaced. Inspections shall be made during and on completion of the mechanical, environmental and endurance tests. Failures observed during these measurements shall count as failed devices.	
2	Internal Visual Inspection	2017	and Condition 'A' of Method 2010
3	Workmanship		See Para 4.9.1.
3a	Radiographic Inspection	2012	
3b	External Visual Inspection	2009	
3c	Physical Dimensions		See detail specification and Para 4.9.1.3 of this specification
4	High Temperature	1008	Condition 'B'. Electrical measurements as specified in the detail specification shall be recorded at 0, 168 and 500 + 48 hours. Total duration of tests shall be 2000 + 96 hours. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded.

TABLE 11 continued on next page.

TABLE 11 - TEST METHODS FOR HERMETIC HYBRIDS (Continued)

No.	Test	MIL-STD-883, Method	Conditions and/or Remarks
5	Operating Life	1005	Conditions as specified in the detail specification. Electrical measurements as specified in the detail specification shall be recorded at 0, 168 and 500 + 24 hrs; 1000 + 48 hrs and 2000 + 48 hrs. Total duration of tests shall be 2000 + 96 hrs. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded
6	Thermal Shock	1011	Condition 'B'; go-no-go electrical measurements after test
7	Thermal Cycling	1010	- ditto -
8	Mechanical Shock	2002	Condition as specified in PSS-01-608
9	Vibration	2007	Condition 'A'; go-no-go electrical measurements after test
10	Constant Acceleration	2001	Condition as specified in PSS-01-608; go-no-go electrical measurements after test
11	Seal	1014	Condition 'A', fine leak; Condition 'C', gross leak
12	Lead Integrity	2004	Conditions B_1 and C_1 as applicable. Measurements: only visual inspection for damage
13	Moisture Resistance	1004	Lead Integrity test is considered as initial conditioning
14	Solderability/ Weldability	2003	All terminations
15	Marking Permanency	2015	

TABLE 11 continued on next page.

TABLE 11 - TEST METHODS FOR HERMETIC HYBRIDS (Continued)

No.	Test	MIL-STD-883, Method	Conditions and/or Remarks
16	Bond Strength/ Adherence (a) Bond Strength (b) Chip Adherence (c) Substrate Attachment Strength	 2011 2019 2027	 Condition 'D'

4.9.2 Thick-Film Chip-Carrier Boards

A thick-film chip-carrier board (CCB) consists of a ceramic substrate carrying surface-mounted devices (SMD) such as chip carriers, chip capacitors and chip resistors with optionally printed resistors. The interconnections are formed by several layers of thick-film conductors.

The testing shall be performed on 15 test structures representative of the technology to be approved.

The size of the substrate shall be the biggest for which approval is sought.

The chip components mounted on the board shall be representative of their size range.

The printed resistors, if used, shall be included in the highest and lowest resistence value.

The number of conductive layers shall be the highest for which approval is sought.

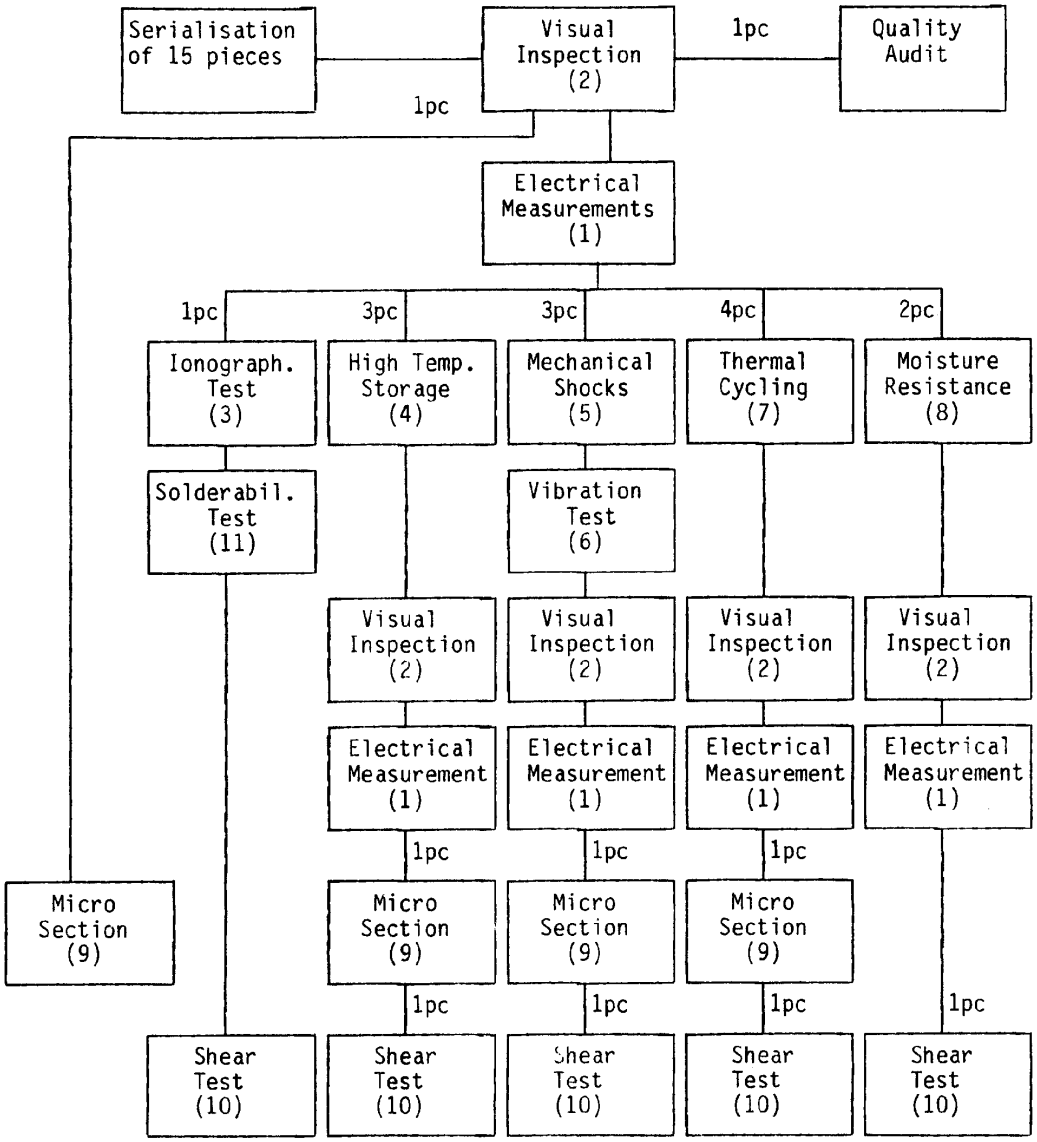
The structure shall be designed in such a way as to allow measurements of all mounted components. In particular, the resistance of the series connection of all solder joints shall be measured.

All electrical measurements to be performed on the structure shall be reported in a detailed specification to be written by the manufacturer and agreed with ESA.

Testing shall be performed in accordance with the test plan shown in Figure 20. No failures are allowed.

Satisfactory test results of reworked test structures shall automatically imply the acceptance of non-reworked test structures.

The structure for Quality Audit shall be sent to ESA together with the results of the initial electrical test.



NOTE: Numbers in parenthesis refer to test numbers in Table 12

FIGURE 20 - TEST PLAN FOR CCBs

TABLE 12 - TEST METHODS FOR CCB's

Test No.	Test Description	Test Method	Conditions/Remarks
1	Electrical Measurements	Detail Spec.	Electrical measurements of all parameters listed in the detail spec. shall be performed in accordance with the test methods specified therein. Parameters measured shall include: Dielectric withstanding voltage and insulation resistance between different conductor layers; Resistance of solder joints, Resistance of conductor interconnections and via's; Printed resistor value and TCR, Chip capacitors: capacitance, tangent delta and insulation resistance.
2	Visual Inspection	MIL-STD-883, Method 2017	As applicable
3	Ionograph Test	MIL-P-28809A	
4	High Temp. Storage	MIL-STD-883, Method 1008	Condition 'B'; T_{amb} = +125° C. Electrical Measurements as specified in the detail specification shall be recorded at 0, 168 and 500 hours. Total duration of tests shall be 2000 hours. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded.
5	Mechanical Shock	MIL-STD-833 Method 2002	Condition 'A'; 500 g; Orientation: Y_1, Y_2, Z_1, X_1.

TABLE 12 continued on next page.

TABLE 12 - TEST METHODS FOR CCB's (Continued)

Test No.	Test Description	Test Method	Conditions/Remarks
6	Vibration	MIL-STD-883 Method 2007	Condition 'A'
7	Thermal Cycling	MIL-STD-883 Method 1010	Condition 'B'; Temperature extremes: -55 and +125°C; 200 cycles in total. Dwell time at each temperature extreme: 15 minutes minimum. Rate of temperature change: 10°C per minute minimum. Electrical measurements and visual inspection shall be performed after 50, 100 and 200 cycles. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded.
8	Moisture Resistance	MIL-STD-202F Method 103B	Condition 'C'
9	Micro-sectioning	-	Microsectioning shall be performed on 1 piece and show: solder joints, via's,insulation and conductor layer.
10	Shear Test	MIL-STD-883, Method 2019	As per detail specification. Alternatively, the torque test may be performed.
11	Solderability Test	MIL-STD-883 Method 2003	All terminations

4.10 TEST REVIEW

4.10.1 Data Presentation

The data files to be prepared for each tested structure shall be entitled "Data File of Capability Approval Testing of .....(part type)" and bear the relevant contract number and date. Each file shall contain:

4.10.1.1 Summary Schedule Sheet(s)

This sheet (or sheets) shall summarize the entire test sequence and include in/out burn-in numbers, scheduled and actual data of each operation and relevant electrical tests (e.g. go-no-go recorded, etc.). The sheet(s) shall be presented such that status can be easily ascertained.

Updated summary sheet(s), showing relevant part type and lot number(s), shall be sent to ESA at each agreed milestone.

4.10.1.2 Equipment Accuracy

The manufacturer shall provide ESA with a list of all equipment to be used and the accuracy thereof, including the applicable calibration controls.

4.10.1.3 Data Records and Histograms

Data records and histograms shall provide all information obtained from the time of burn-in up to and including end of test. Any data related to the Subgroup Control Devices shall also be included. Each recorded parameter shall be marked with a symbol and listed together with the pertinent measurement conditions and limits.

Where a parameter drift requirement is specified, the data shall include both drift percentage and absolute change. The same information shall be provided in respect of parameters measured during life testing, even if no parameter drift criteria are applicable during such testing. The manufacturer shall supply histograms of the measured parameters, containing all records from time of burn-in up to and including end of testing as well as the average sigma and two sigma. If parameter drift is specified, a histogram of the percentage and/or absolute drift shall be included.

4.10.1.4 Other Requirements

The test review data shall include an index and any relevant comments and graphs.

4.10.2 Failure Criteria and Classification

Failures of any of the categories specified in the following subparagraphs shall contribute towards failure. Each part exhibiting a failure of any of these categories shall count as one failure.

4.10.2.1 Visual and Mechanical Inspection

These inspections form part of the Quality Audit procedure. The detection of any defective units at this stage may be cause for verification of the entire lot, the replacement of defective parts or the suspension of testing and ordering of a new lot. Such defective parts shall be considered as rejects and contribute towards lot acceptance/rejection.

4.10.2.2 Out-of-Tolerance Parameters

These parameters shall be measured during the initial electrical tests. Defective units shall not be submitted to qualification testing. Any

defects noted during subsequent electrical measurements shall be considered as rejects and contribute towards lot acceptance/rejection.

4.10.2.3 Degradation

This applies to those parameters that, following the original measurement, exceed the specified limits when subsequent measurements are performed. Any devices whose parameters do not conform to the specified limits shall be considered as rejects.

If the relevant detail specification prescribes delta values for a particular parameter, the applicable limit shall be the absolute limit plus or minus the appropriate delta limit.

4.10.2.4 Parameter Drift

Devices whose parameter drift exceeds the limits defined in the detail specification shall be considered as rejects and contribute towards failure. Even if no accept/reject criteria are specified, ESA reserves the right to suspend the approval of test results in the event of sudden large parameter changes and/or anomalous behaviour for which no reasonable explanation can be given.

4.10.2.5 Catastrophic Failures

This type of failure occurs when parameters exceed the specified limits to such an extent that a device is rendered ineffective. Catastrophically failed devices shall be considered as rejects.

4.10.2.6 Operator Errors

These are failures caused by electrical or mechanical overstress which, normally, do not contribute towards failure. However, when a failure of this category is detected, the testing of the subgroup concerned shall

cease immediately and the manufacturer shall notify ESA without delay. The manufacturer shall then take appropriate action to determine the cause of failure and, when established, satisfy ESA that such cause has been isolated and remedied. ESA will then decide in the light of all available evidence whether or not those parts that may have suffered overstress are to be replaced. Any replacement parts shall be submitted to all of the tests which the replaced parts have undergone. Replacement parts shall always be from the same production lot as the original parts and must have been processed identically.

4.11 CAPABILITY APPROVAL

Capability approval status will be granted by ESA authority upon satisfactory completion of Evaluation and Capability Approval testing and will be valid for two years.

5. MAINTENANCE, SUSPENSION AND WITHDRAWAL OF CAPABILITY APPROVAL

5.1 MAINTENANCE OF CAPABILITY APPROVAL

Capability approval is maintained by the continuous production of devices according to the technology defined in the PID. At least two months prior to the expiry date of line approval, the manufacturer shall furnish ESA with the following details of lots processed to ESA Specification PSS-01-608: lot numbers; deliverable parts and numbers and a synthesis of failures during burn-in, environmental and life testing. If considered necessary, ESA may require further details.

The minimum requirement for capability approval is that, during the last 12-month lapse period, one lot of hybrids has been manufactured, screened and tested for lot acceptance in accordance with ESA PSS-01-608 with the addition of mechanical tests of Subgroup I of the test plan shown in Fig. 19 of this specification.

Renewal of capability approval shall be valid either from the date on which:

a) the previous approval expired or,

b) the date on which lot acceptance testing was completed successfully if this date occurred more than 6 months prior to (a).

In addition, the manufacturer shall provide ESA with three samples of a recently manufactured hi-rel batch of components for Destructive Physical Analysis (DPA). On the basis of both the information received and the DPA results, ESA will then decide whether approval can be maintained.

In case of any deviations from the qualified technology, i.e. if new materials and/or processes are to be introduced, ESA and the

manufacturer will jointly agree on a testing programme which will cover the new techniques and serve for approval maintenance purposes.

5.2 SUSPENSION OF CAPABILITY APPROVAL

ESA may suspend the approval status of a production line, or any part thereof, for the following reasons:

a) failure(s) which cannot be remedied within a reasonably short period of time;

b) failure of more than two consecutive lots.

In the event of (a) and (b), the manufacturer shall initiate any corrective action considered appropriate and, to achieve reinstatement of approval status, supply ESA with evidence that the cause of failure has been eliminated.

During the suspension period, the line shall not be considered as approved and not be used for the production of circuits unless they serve for approval purposes.

5.3 WITHDRAWAL OF CAPABILITY APPROVAL

Approval status will be withdrawn:

a) at the request of the manufacturer,

b) in case of persistent non-adherence to the production processes agreed for capability approval.

ANNEX A - DEFINITIONS

Chip Component

A component in its ultimate state of miniaturisation.

Component

A device which performs an electronic, electrical or electromechanical function and consists of one or more elements joined together which, normally, cannot be disassembled without destruction. The terms component and part are interchangeable. Typical examples of components are: transistors, integrated circuits, hybrids, capacitors, etc.

Destructive Physical Analysis (DPA)

A series of inspections, tests and analyses of a sample component to verify that the materials, design and workmanship used for its construction as well as the construction itself meet the requirements of the applicable specification and are suitable for the intended application.

Deviation

A written authorisation to accept a specific item which, during production or after inspection, has been found to deviate from the applicable requirements, but is nevertheless considered to be suitable for "use-as-is" or after "rework" by an approved method.

Film Network

Layers of conductive, resistive, dielectric and/or passivating materials deposited onto an insulating substrate for the purpose of performing electronic circuit functions.

ANNEX A (Continued)

Hybrid Microcircuit

A component performing an electronic circuit function which consists of a thick or thin film network on a substrate which supports active and/or passive chip components connected to it.

Limited Life Material

A material which can be processed and stored for only a limited period of time before deterioration of its specified properties.

Nonconformance

An apparent or proven condition of any item or document that does not conform to the specified requirements and may lead to incorrect operation or interpretation during its envisaged usage. The term "nonconformance" is also used for failure, discrepancy, defect, anomaly, malfunction and deficiency.

Process Identification Document (PID)

A set of frozen documents defining the technology, processes and inspection procedures applicable to the manufacture of the components or items on order.

Production Lot

A production lot consisting of a quantity of a specific device type manufactured on the same production line by the same processing techniques and according to the same component/part design using the same raw materials during one uninterrupted production run.

ANNEX A (Continued)

Selected Sublot

A selected sublot is that part of a production lot which is manufactured in excess of the actual quantity of components required.

Symbols and Abbreviations

The symbols and abbreviations defined in MIL-S-19500, MIL-M-38510, MIL-STD-883, ESA Specifications PSS-01-60, PSS-01-606, this specification and the applicable detail specifications shall be applicable.

Thick Film

A network onto which the film is deposited by screen-printing methods. The thickness of the fixed film is usually in the range of 10 to 25 micrometres.

Thin Film

A network onto which the film is deposited by one or more of the following processes: electro-depositing, plating, evaporation, sputtering, anodisation or polymerisation. The thickness of the film may be in the range of 50 to 2000 Angström.

Traceability

To derive from recorded identification data the history, application, use and location of an item.