ESA PSS-01-301 Issue 2
April 1992

european space agency
agence spatiale européenne

Derating requirements applicable to electronic, electrical and electro-mechanical components for ESA space systems

Prepared by:
Product Assurance & Safety Department
European Space Research and Technology Centre
Noordwijk, The Netherlands

Approved by:
The Inspector General, ESA

ESA PSS-01-301 Issue 2
April 1992

Derating requirements applicable to electronic, electrical and electro-mechanical components for ESA space systems

Prepared by:
Product Assurance & Safety Department
European Space Research and Technology Centre
Noordwijk, The Netherlands

Approved by:
The Inspector General, ESA

european space agency / agence spatiale européenne
8-10, rue Mario-Nikis, 75738 PARIS CEDEX, France

Published by ESA Publications Division,
ESTEC, Noordwijk, The Netherlands

Printed in the Netherlands.

ESA Price Code: E1

ISSN 0379-4059

ABSTRACT

Electronic, electrical, and electro-mechanical components used in equipment for use on ESA spacecraft shall be suitably derated according to the requirements given herein and shall observe the application rules given in this document.

Suitable derating is decided on the analyses described hereafter.

The tables of this document contain:

- the derating to be applied to specified component parameters
- the parameter degradations to be used for worst case analysis
- notes to the tables containing application rules for the components

Data is not supplied for radiation effects analysis as this varies widely and must be considered on a case-by-case basis.

DOCUMENT CHANGE RECORD

Issue number and date	Sections affected	Remarks
Issue 1 December 1982		
Issue 2	All sections	Document completely revised

PAGE INTENTIONALLY LEFT BLANK

SECTION 1. SCOPE

Electronic, electrical, and electro-mechanical components used in equipment for use on ESA spacecraft shall be suitably derated according to the requirements given herein and shall observe the application rules given in this document.

Suitable derating is decided on the analyses described hereafter.

The tables of this document contain:

- the derating to be applied to specified component parameters
- the parameter degradations to be used for worst case analysis
- notes to the tables containing application rules for the components

Data is not supplied for radiation effects analysis as this varies widely and must be considered on a case-by-case basis.

PAGE INTENTIONALLY LEFT BLANK

SECTION 2. DERATING

Derating is the intentional reduction of electrical and thermal stress in order to increase the useful lifetime of a component.

The total derating to be applied to a component is established after the following analyses have been performed :

- Parameter derating;
- Worst case analysis;
- Radiation effects analysis.

These analyses are described in the following sections.

2.1. Parameter derating

The first part of the table for each category of component in Section 5 gives a derating figure to be applied to those component parameters which have a rated value specified in the procurement/Detail Specification; this is usually given as a percentage of the rated value.

Transient or "Surge" conditions shall be taken into account where applicable, and derating determined as follows :

- when the procurement specification includes parameter values for transient or surge conditions, then the same derating figures as for steady state equivalent parameters shall be used, unless otherwise specified,
- when transient or surge conditions are applicable, but no transient or surge values are specified, then it must be assured that the transient or surge values are below the steady state values of the procurement specification.

2.2. Worst-case analysis

The second part of the table for each category of component in Section 5 gives various parameter degradations which are to be used in the worst-case analysis. These figures are valid for mission times up to ten (10) years and assume that the components are already derated as per Section 2.1 and used in accordance with the application rules given in the notes to the tables.

Where components are required to operate in a protection mode or in a fail-safe mode in order to prevent failure propagation (e.g. short-circuit protection), the components concerned shall meet the derating requirements and application rules when performing the protection or fail-safe function under the worst failure case (i.e. highest stress applied to the components).

The worst-case analysis shall include :

- drift from initial tolerances, temperature effects, ageing effects: the figures for these effects are included in the tables,
- any operational modes that may induce excess stress and any failure mode which must be contained and controlled: additional margins/derating/parameter degradation other than those in the tables, shall be considered as necessary.

Several effects may be additive, e.g. the drift values given in the tables have to be added to the initial tolerance and to the temperature-coefficient effect. Radiation effects may be similarly additive.

2.3. Radiation effects

Unless it is known that the components under consideration are sufficiently radiation tolerant for the foreseen application environment, a radiation effects analysis shall be performed to identify consequent parameter degradation.

The results of this analysis shall form the basis for any additional derating that may be required, either as a modification of the derating figures for the rated parameters, or as an additive constituent in the worst-case analysis.

In the case of semiconductor devices, the radiation effects analysis shall cover:

- parameter degradation due to total dose effects such as increase in leakage current, threshold or offset voltage shift ...
- heavy ion or proton induced effects ("single event upset") which may cause transitory malfunction such as "bit-flips", (semi-)permanent damage such as latch-up, or catastrophic failure such as "burn-out".

SECTION 3. APPLICABILITY & COMPONENT SELECTION

The requirements of this document are applicable to all components for use on ESA space systems. Such components shall be selected in accordance with the policy defined in ESA PSS-01-60.

For components not covered by these derating requirements, the designer shall, in addition to seeking approval for the use of component types as required by ESA PSS-01-60, propose derating requirements and application rules in a manner similar to the presentation in this document. The proposal shall be supported by test data for the component types concerned. (N.B. ESA PSS-01-60 requires a component evaluation to be undertaken as the basis for approval: such an evaluation should provide the necessary data for the requirements of this document to be implemented).

If, for any reason, the requirements of this specification cannot be implemented, a waiver request shall be issued with appropriate justification.

Application of derating requires the proper assessment of component operating conditions through design analysis, including worst-case analysis.

The derating requirements must be taken into consideration sufficiently early in the design cycle for any consequential design trade-offs to be made. Specific attention must be paid to breadboards, engineering models, etc., where derating of components may not have been considered. Their use in flight hardware must include a proper rating/derating/assessment and redesign if needed.

PAGE INTENTIONALLY LEFT BLANK

SECTION 4. APPLICABLE DOCUMENTS

The following documents are applicable to the extent specified herein:

ESA PSS-01-30	Reliability assurance requirements for ESA space systems.
ESA PSS-01-60	Component selection, procurement and control for ESA space systems
ESA PSS-01-603	ESA preferred parts list

PAGE INTENTIONALLY LEFT BLANK

SECTION 5. TABLES FOR DERATING AND WORST CASE ANALYSES

Contents:

ABBREVIATIONS AND SYMBOLS

ABBREVIATIONS

A/D	Analogue to Digital
AWG	American Wire Gauge
CMOS	Complementary Metal Oxide Semiconductor
D/A	Digital to Analogue
FMECA	Failure Modes, Effects and Criticality Analysis
I^2L	Integrated Injection Logic
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Channel Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
UHF	Ultra-High Frequency
VHF	Very-High Frequency

SYMBOLS

ΔC	Change in capacitance value
ΔR	Change in resistance value
I	Current
I_F	Forward current
I_R	Rated current
P_{max}	Rated power at +25°C
t	Time
T_{amb}	Ambient temperature (temperature of the mounting board near to the component)
T_{case}	Case temperature
T_j	Junction temperature
$T_{op(max)}$	Maximum operating temperature (case temperature unless otherwise stated)
$V_{BE(sat)}$	Base-to-emitter saturation voltage
$V_{CE(sat)}$	Collector-to-emitter saturation voltage
$V_{CE(max)}$	Maximum collector-to-emitter voltage

SECTIONS

01 Capacitors

02 Connectors

03 Crystals

04 Diodes

05 Filters

06 Fuses

07 Inductors, transformers, chokes, motor windings

08 Microcircuits

09 Relays and switches

10 Resistors and flexible heaters

11 Thermistors

12 Transistors

13 Wires and cables

14 Miscellaneous:
- Opto-electronics devices
- RF passive components

Component type		Rated voltage derated to	Maximum operating temperature	Remarks	WORST-CASE ANALYSIS ΔC to be added to the initial tolerance and to the temperature coefficient effect.	
Ceramic, fixed	Temperature compensated	50%	+85°C		±1.5%	50% drop in initial minimum insulation resistance to be considered.
Discrete and chips (2)	General purpose	50%	+85°C		+25%, -20%	
Glass, porcelain		50%	+85°C		±0.2% or ±0.5 pF whichever is greater.	
Mica		50%	+85°C		±0.5%	
Metallised plastic film CRH (1) & (2) MKU, CHS (2)		50%	+85°C		±2%	50% drop in initial insulation resistance.
Solid tantalum, (2) Encapsulated and chips		60% 60%	+50°C +85°C	See Notes 3 & 5 See Notes 4 & 5	±10%	100% increase of the initial maximum leakage current to be considered.
Non-solid tantalum (2) (Wet slug)		50%	+75°C	Surge voltage also derated to 50%	±15%	Dissipation factor: 100% increase of the initial maximum limit. DC leakage current: 50% increase of the initial maximum limit.
Solid aluminium		50%	+85°C		±10%	Tg ∂: 20% Increase of initial maximum limit.
Variables		50%	+85°C		±5%	

Notes: (1) Recommended minimum energy to be considered for correct self-healing: 500 microjoules.
(2) Ripple and surge current and voltage shall be derated to 75% of the rated values.
(3) With circuit impedance comprised between 0.1 and 1 Ω/Volt.
(4) With circuit impedance greater than 1 Ω/Volt.
(5) These capacitors shall not be used in power supply filters.

PAGE INTENTIONALLY LEFT BLANK

Maximum applied voltage	: Derate to 50% of specified voltage at altitude (pin to pin and pin to shell).
Maximum temperature	: 30°C below the specified maximum operating temperature.
Maximum current (2) per contact	: 50% of rated current specified in the procurement specifications and additionally, as specified for the wires & cable attached to them.
Maximum mating and and demating cycles (1)	: 50
Degradation to be considered during worst-cas analysis	: No degradation

Notes:

(1) Saver connectors shall be used during integration to lower number of mating and demating cycles. The number of mating/demating for that end of a saver connected to the Hi-Rel connector is also limited to 50.

(2) For power connectors, power and return lines shall be separated by at least one unassigned connector contact to reduce short circuit risk.

(3) When multi-pin connectors are close to one another, they shall be configured such that mating with a wrong connector is not possible or the contact assignments shall be chosen such that mating with a wrong connector will not cause damage to the unit itself or to any other element of the system.

PAGE INTENTIONALLY LEFT BLANK

Rated drive level	:	Shall never be exceeded.
Operating temperature	:	10°C higher than the minimum specified value. 10°C lower than the maximum specified value.
Worst-case analysis	:	4 times the frequency shift specified in the procurment specification.

PAGE INTENTIONALLY LEFT BLANK

Specified minimum power	Derate to 50%
Specified maximum reverse voltage	Derate to 75%
Specified maximum current (for T_{amb} = +25°C)	Derate to 60% (Note 1)
Maximum junction temperature	+110°C
WORST-CASE ANALYSIS	Drift to be considered.
Leakage currents: Breakdwon voltages: Forward voltages:	5 times the specified maximum. 5% decrease of the specified maximum. 10% increase of the specified maximum.
Zener voltage regulators and reference diodes shall be used at the minimum current compatible with stable operations.	

Notes:

(1) The value of the current shall be calculated with the following formula: $I_{F(derated)} = 0.6 I_{F(max)} \left(1 - \frac{T_1 - T_2}{110 - T_2}\right)$

Where: For small signal diodes operating without heat sink (measurement of T_{case} impractical), the following rule of thumb is applicable, where T_{amb} is the temperature of the mounting board:

T_2 = +25°C

$T_1 = T_{amb}$ for T_{amb} > +25°C or +25°C for $T_{amb} \leq$ +25°C

For diodes operating with heat sink: $T_2 = 0.6$ (T_m +25°C)

T_m = maximum case temperature at which manufacturer allows max. current

$T_1 = T_{case}$ for $T_{case} \geq T_2$ or T_2 for $T_{case} < T_2$

(2) For LED's, see Opto-electronic devices in the Miscellaneous section.

PAGE INTENTIONALLY LEFT BLANK

Component type	Rated voltage derated to	Maximum case temperature	Remarks	WORST-CASE ANALYSIS To be added to the initial tolerance
E.M.I. filters	50%	+85°C	Feed-through current to be derated to 50%	Attenuation degradation of 2 dB

PAGE INTENTIONALLY LEFT BLANK

1. Fuses shall be avoided whenever possible.
2. Where fuses are needed, cermet fuses shall be used.
3. The largest fuse rating compatible with the source current capability shall be used.
4. Derating factor of rated current: 50%. (The power supply shall be capable of delivering 4 times the specified fuse rated current in order to obtain short fusing times).

PAGE INTENTIONALLY LEFT BLANK

Maximum applied voltage:	Derate to 50% of the rated dielectric withstanding voltage between windings and between windings and case. (1)
Maximum operating temperature:	This temperature results from the combined effects of hot spot temperature, the ambiant temperature, and the temperature rise resulting from Joule heating. It shall be less than 75% of the rated operating temperature.
Wire insulation grade:	Higher than +130°C.
Degradation to be considered: in worst-case analysis	No degradation.

Notes: (1) For voltages greater than 200 Volts, the maximum applied voltage (ac peak, dc or combined) shall be less than 0.77 x ac partial discharge test level.

PAGE INTENTIONALLY LEFT BLANK

Parameters	Logic circuits		Microprocessors, peripherals & memories			
	Bipolar	CMOS family 4000	CMOS	TTL	NMOS	I^2L
Maximum junction temperature Maximum case temperature	+110°C + 85°C					
Specified rated supply voltage	±5%	Derate to 90%	±5%	±5%	±5%	–
Specified rated supply current	–	–	–	–	–	±3%
Specified rated power dissipation at T_{case}	Derate to –	80%	Derate to –	Derate to 75%	Derate to 75%	Derate to –
Specified maximum frequency	90%	90%	90%	90%	90%	90%
Specified rated output current or fan-out	80%	80%	80%	80%	80%	80%
Specified rated input voltage	–	–	–	–	–	–
WORST-CASE ANALYSIS: No degradation beyond the minimum specified input and output voltage range to be considered.						

Notes:

(1) The derating of Hybrid microcircuits shall be based on the derating of individual chip components and the assembly technique used.

(2) Number of Erase/Write cycles for EEPROM's shall be determined by an evaluation.

PAGE INTENTIONALLY LEFT BLANK

	LINEARS				INTERFACE				
Parameters	Op Amp	Compa-rators	Regulators	Analogue switches	A/D converters	D/A converters	Line receiver	Line drivers	Analogue switches
Max. junction temperature	+110°C								
Maximum case temperature	+85°C								
Specified rated supply voltage	Derate to 80%	Derate to 90%	Derate to –	Derate to 90%	±5%	±5%	±5%	±5%	Derate to 90%
Specified rated power dissipation	75%	75%	75%	75%	Derate to 80%	Derate to 80%	Derate to 80%	Derate to 80%	80%
Specified max. frequency	90%	–	–	90%	90%	90%	90%	90%	–
Specified rated output current	80%	80%	80%	80%	–	–	80%	80%	90%
Specified rated input voltage	70%	–	90%	–	–	–	–	–	–

WORST-CASE ANALYSIS
The following changes will be considered:

1mV of input offset voltage (operational amplifiers and comparators)
25% of voltage gain (operational amplifiers)
0.25% in output voltage (voltage regulators)
0.20% load regulation (voltage regulators)

08 MICROCIRCUITS (Continued)

PAGE INTENTIONALLY LEFT BLANK

Contact voltage	: No derating
Coil voltage	: No derating
Number of operations (1)	: See derating curve on next page
Contact current (2) (3)	: See derating curve on next page
Derate to 50% of inductive load rating or 40% of resistive load rating if inductive load rating is not specified. Derate to 50% of motor load rating or 20% of resistive load rating if motor load rating is not specified. For filament, derate to 10% of resistive load rating.	
Contact current transients (4)	: Shall be limited such that $I^2t \leq 16. (I_R)^2. 10^{-5}$ (A^2s)
Degradation to be considered for worst-case analysis	: An increase of 4 times the limit specified for contact resistance shall be used for more than 1000 switching operations (5)

Notes:

(1) If the number of operations is below 50 (including integration and testing) :
For relays with $I_{overload} = 2I_R$, I_R may be used,
For relays with $I_{overload} = 4I_R$ or more, 2 X I_R may be used,

(2) It is not recommended to use a relay with a main contact current below 20% of the rated current, except for low-level application (< 1 mA) where the smallest current rated relay shall be used.

(3) Contacts may be paralleled for redundancy, but the use of paralleled contacts does NOT increase contact current rating over the value specified for a single contact.

(4) In the case where the pulse duration is lower than or equal to 10 microseconds, the transient current shall be limited to 4 X I_R. If outside these formulae, consideration on a case by case basis.

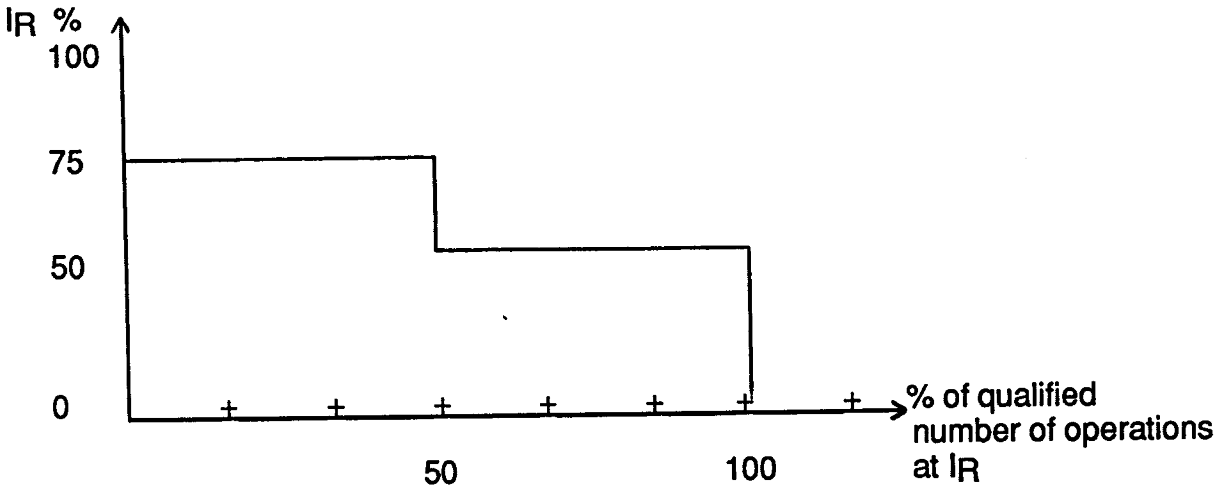
(5) For a number of switching operations less than 1000, an increase of twice the contact resistance shall be used.

(6) Suppression diodes inside relays shall not be used.

PAGE INTENTIONALLY LEFT BLANK

The same derating and WCA requirements as for relays (except coil voltage) shall be used.

Note 1 : A 4°C minimum dead band shall be required and
a temperature rate of change equal to or greater than 0.11°C per minute shall be used.

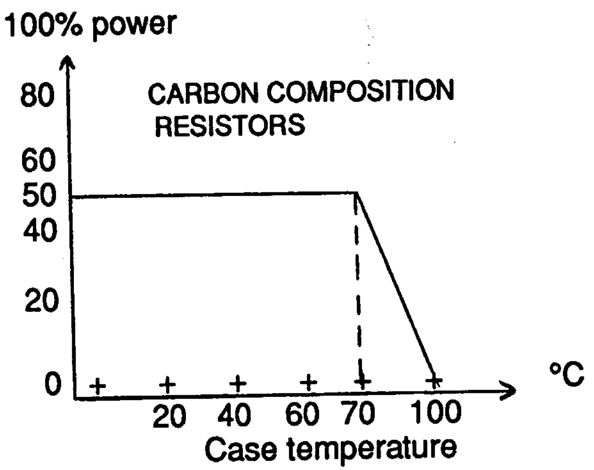


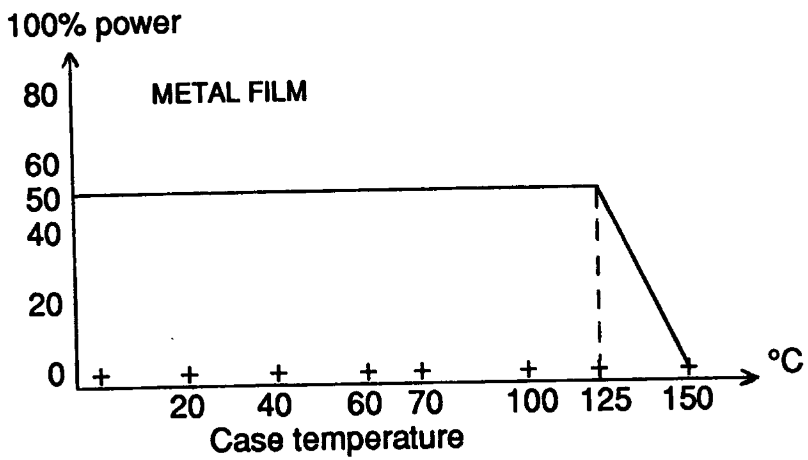
CURRENT DERATING CURVE FOR RELAYS AND SWITCHES

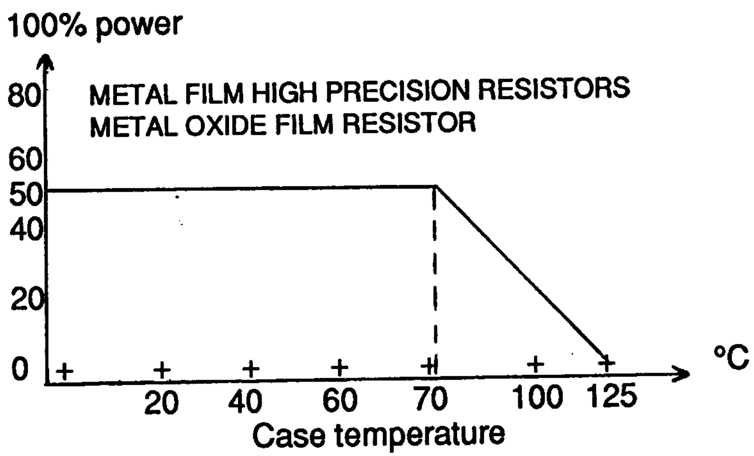
PAGE INTENTIONALLY LEFT BLANK

Component type	Rated voltage derated to	Rated power derated to	Allowed max. case temperature at derated power	Zero power maximum case	WORST CASE ANALYSIS ΔR to be added to the initial tolerance and to the temp. coeff. effect at derated power
Carbon composition (RCR)	80%	50%	+70°C	+100°C	±15%
Metal film (RNC)	80%	50%	+125°C	+150°C	±2%
Metal oxide film (RLR)	80%	50%	+70°C	+125°C	±4%
Film high precision (RNC90 - RS92)	80%	50%	+70°C	+125°C	±0.1%
Wire wound power incl. chassis (RWR, RER)	80%	50%	+25°C	+175°C	±1.5%
Wire wound precision (RBR) Tol. 1%	80%	50%	+125°C	+130°C	±0.4%
Tol. 0.5%		35%			
Tol. 0.1%		25%			
Chips	80%	50%	+25°C	+100°C	±2%

PAGE INTENTIONALLY LEFT BLANK

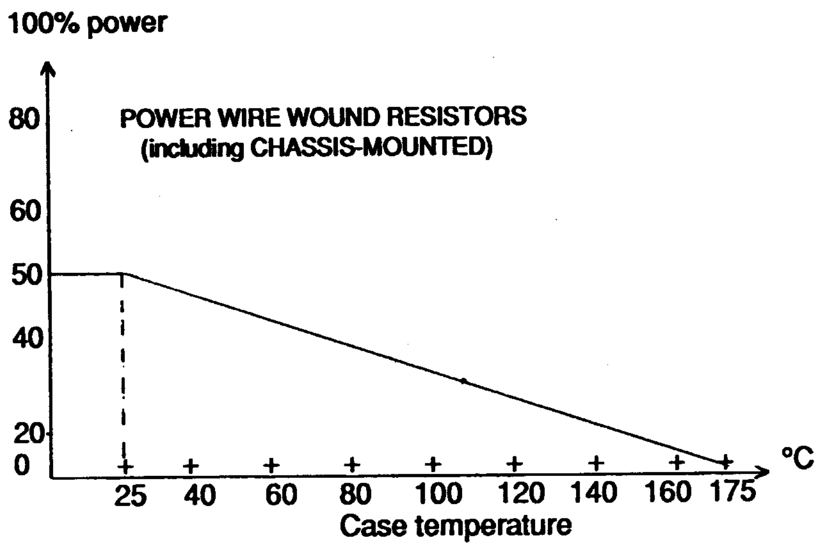


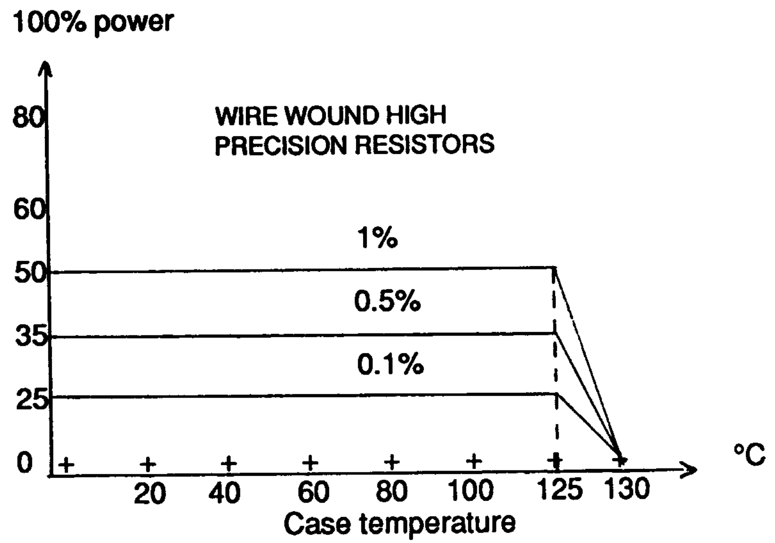


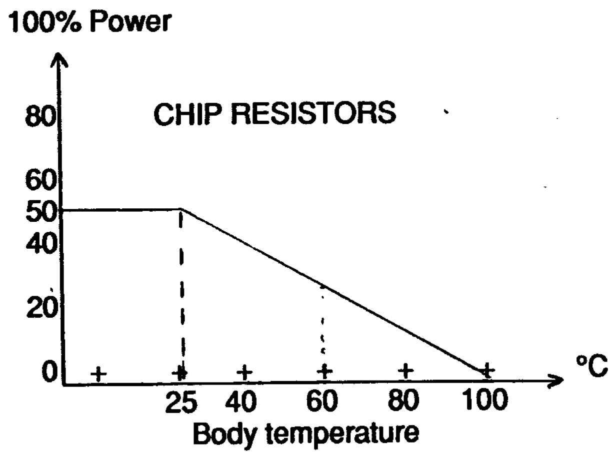


10 RESISTORS AND FLEXIBLE HEATERS (Continued)
10.1 RESISTORS

PAGE INTENTIONALLY LEFT BLANK







10 RESISTORS AND FLEXIBLE HEATERS (Continued)
10.1 RESISTORS

PAGE INTENTIONALLY LEFT BLANK

10 RESISTORS AND FLEXIBLE HEATERS (Continued)
10.2 FLEXIBLE HEATERS

Component type	Specified rated power per unit area derated to	WCA: ΔR to be added to the initial temperature tolerance and to the temperature coeff. effect at derated power
Flexible heaters	50%	±5%

PAGE INTENTIONALLY LEFT BLANK

Power derating:	Derate to 50% of the power necessary to give an error of resistance value equal to the initial tolerance.
Voltage derating between thermistor element and mounting base:	Derate to 50% of the specified rated dielectric withstanding voltage.
Degradation to be considered for worst-case analysis:	±2% of the resistance value in addition to the initial tolerance.

PAGE INTENTIONALLY LEFT BLANK

Minimum specified reverse voltage:	Derate to 75%	(Note 2)
Maximum specified current:	Derate to 75%	
Maximum specified power:	Derate to 60%	(Note 1)
Maximum junction temperature:	+110°C	(Note 1)
WORST-CASE ANALYSIS	Drift to be considered	
Leakage currents	: 5 times the specified maximum	
Breakdown voltages	: 5% decrease of the specified minimum	
Forward voltages	: 10% increase of the specified maximum	
Gain	: 25% decrease of the specified maximum	
Saturation voltages $V_{CE(sat)}$, $V_{BE(sat)}$	: 10% increase of the specified maximum	
Currents and voltages shall be maintained at levels compatible with the safe operating area.		

Note (1) Detailed calculations permitting compliance with these two requirements are given on the next page.

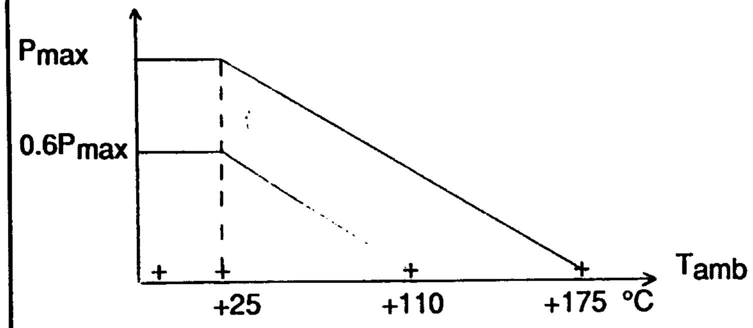
Note (2) For N channel power MOSFET's, susceptibility to heavy ion induced 'burn-out' needs additional derating. To be analysed depending on the technology and the application environment. Worst-case analysis to be considered for each application.

Note (3) For photo-transistors, see Opto-electronic devices in Miscellaneous.

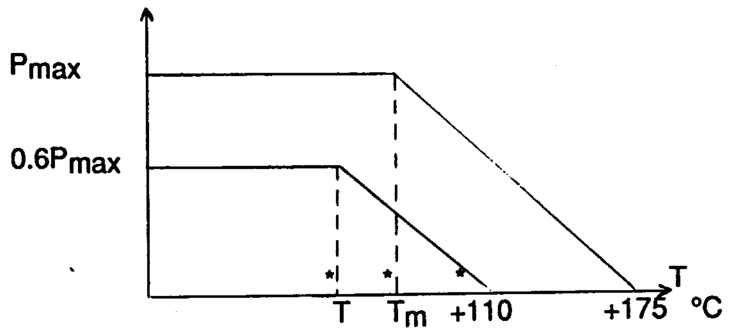
PAGE INTENTIONALLY LEFT BLANK

For small signal transistor operating without heat sink (measurement of T_{case} impractical), the following rule of thumb is applicable, where T_{amb} is the temperature of the mounting board:	$P_{derated} = 0.6 \frac{(110 - T_{amb})}{90} . P_{max}$	$T_{amb} > +25°C$
	$P_{derated} = 0.6 P_{max}$	$T_{amb} \le +25°C$
For transistors operating with heat sink:	$P_{derated} = 0.6 P_{max}$	if $T_{case} \le +110°C - 0.6(175 - T_m)$ °C (Note 4)
	$P_{derated} = \frac{110 - T_{case}}{175 - T_m} P_{max}$	if $T_{case} > +110°C - 0.6(175 - T_m)$ °C (Note 4)

Where T_m= max. specified case temperature at rated power.



Without heat sink



With heat sink
$T = +110°C - 0.6(175 - T_m)$ °C (note 4)

Note 4: The power derating curves and formulae above are based on a maximum T_j capability of 175°C demonstrated during qualification and lot acceptance testing. For types where testing is conducted at lower T_j, the power allowed shall be reduced accordingly to preserve the same 65 °C margin between T_j operating and T_j qualification.

PAGE INTENTIONALLY LEFT BLANK

Maximum applied voltage:	Derate to 50% of the specified maximum insulation voltage (3)														
Maximum applied current versus the wire size in a maximum ambient temp. of 85°C (1) (2)	Wire size AWG	30	28	26	24	22	20	18	16	14	12	10	8	6	4
	Max. current (single wire) in amperes	1.3	1.5	2.5	3.5	5.0	7.5	10.0	13.0	17.0	23.0	32.0	45.0	60.0	81.0

Notes:

(1) When wires are bundled, the maximum design current for each individual wire shall be derated according to the formulae:

$$I_{bw} = I_{sw} \times \frac{29 - N}{28} \quad \text{for } 1 < N \leq 15.$$

or $I_{bw} = 1/2\ I_{sw}$ for $N > 15$.

I_{bw} = maximum current for individual wire in a bundle.

I_{sw} = maximum current for a single wire as given in the table above.

N = number of wires in the bundle.

(2) The current in wires terminated on, or run through, connectors may be restricted further than indicated above by the virtue of the connector contact size.

(3) For High Voltage cables, the maximum ac voltage or ripple shall not exceed 5% of the dc rating and the minimum bend radius for Teflon insulation shall be 5 times the manufacturer's figure.

PAGE INTENTIONALLY LEFT BLANK

Component	Parameters to be derated to:
Light emitting diode	20% of I_{max} but in general any reduction in injection current will improve reliability
Photo-transistor	60% of P_{max} 75% of $V_{CE(max)}$ Junction temperature ≤ +110°C
Optocouplers	20% of I_{max} for the diode 50% of nominal power for the transistor 75% of $V_{CE(max)}$ Junction temperature ≤ +110°C
Charge coupled devices (CCD's)	$T_{amb(max)}$ +75°C
Laser diodes	75% of optical output power $T_{op(max)}$: +30°C for Al GaAs diodes $T_{op(max)}$: +20°C for In GaAs diodes

PAGE INTENTIONALLY LEFT BLANK

Component	Parameters to be derated to:	WORST-CASE ANALYSIS
RF attenuators (1)	50% of recommended Input power	± 0.1 dB to be added to initial attenuation tolerance
RF loads (1)	50% of recommended Input power	± 2% to be added to initial V.S.W.R. (Voltage Standing Wave Ratio)
RF couplers and RF power dividers (1)	50% of RF power	± 0.1 dB to be added to initial amplitude balance tolerance
Circulators and isolators (1)	50% of input power	No degradation

Note: (1) Multipaction: 6 dB minimum power margin.

PAGE INTENTIONALLY LEFT BLANK