DATA ITEM DESCRIPTION

Form Approved
OMB No. 0704-0188

1 TITLE	2 IDENTIFICATION NUMBER
Diagnostic Test and Failure Analysis of Microelectronic Devices (VHSIC/VLSI/MIMIC)	DI-QCIC-81201

3. DESCRIPTION / PURPOSE

3.1 The purpose of the Diagnostic Test and Failure Analysis of Microelectronic Devices (VHSIC/VLSI/MIMIC) is to provide data on automated diagnostic tests to verify failure and causes of failure of microelectronic devices using an internal nodal probe system. Acquired information is intended to allow the successful stimulation of these devices to verify failure, to localize ... (Continued on Page 2)

4 APPROVAL DATE (YYMMDD)	5. OFFICE OF PRIMARY RESPONSIBILITY (OPR)	6a DTIC APPLICABLE	6b GIDEP APPLICABLE
910503	A/SLCET-RE		

7. APPLICATION / INTERRELATIONSHIP

7.1 This Data Item Description contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated in the contract.

7.2 The acquired data will be used to perform test and diagnostics on microcircuit devices using a computer-aided diagnostic E-beam test (CADET) system or some other suitable internal nodal probe system. (Continued on Page 2)

8 APPROVAL LIMITATION	9a. APPLICABLE FORMS	9b AMSC NUMBER
		A6126

10. PREPARATION INSTRUCTIONS

10.1 Reference Documents. The applicable issue of the documents cited herein, including their approval dates and dates of any applicable amendments, notices and revisions, shall be as specified in the contract.

10.2 Data requirements. The data to be acquired for automated microcircuit diagnostics and probing shall include device design/layout on chip interconnects, input/output test patterns, electrical and timing requirements, simulation methodology, package design/layout, and environmental requirements. For test and analysis of these devices, the following items shall be delineated to verify and determine failure causes:

a. electrical characteristics
b. mechanical characteristics
c. environmental characteristics
d. reliability characteristics
e. microcircuit and associated block diagrams
f. functional description of circuit operation

(Continued on Page 2)

DISTRIBUTION STATEMENT

DISTRIBUTION STATEMENT A: Approved for public release; distribution is unlimited.

Block 3, Description/Purpose (Continued)

the cause of failure, and to transfer it in an acceptable format utilizing a standard type electronic media. Diagnostic results will be used for appropriate corrective action.

Block 7, Application/Interrelationship (Continued)

7.3 The data requirements necessary to perform suitable tests are to be compatible with or part of the VHSIC Hardware Description Language (VHDL).

Block 10, Preparation Instructions (Continued)

10.3 Format. The following data formats shall be provided as follows:

a. The layout (topological) information shall be in standard Caltech Intermediate Format (CIF) from the Computer-Aided Design (CAD) database on magnetic media (cartridge, tape or disk) (see MIL-STD-1840A). Functional blocks shall be labeled and described including signal, ground, power, and clock lines. The information shall be suitable for directing the positioning of a prober (E-beam) to a given location for acquisition of signals on the internal nodes of the device. Simulation information shall be available or extractable from the CAD database to verify the proper operation of the nodes being probed and shall be sufficient to allow simulation of the nodal response to external stimuli.

b. Input functional test vectors, corresponding output vectors, timing delays, clock and data speeds, and voltage/current/power parameters shall be provided in ASCII format on disks,cartridge (TK-50), or 9-track magnetic tape (1600 bpi, unlabeled, fixed record length) with vectors labeled, pins identified, and a format character description so devices can be properly exercised and tested for compliance to specified performance. The format of this test vector (ASCII format) shall be suitable for translation into required format used by Automatic Test Equipment (ATE) such as programmable logic analyzers/generators and generic IC verification test systems. Modified test patterns (MTP) shall be provided in order that a more efficient set of test vectors for failure verification and failure cause(s) can be used.

Block 10, Preparation Instructions (Continued)

c. The results of circuit critical path analysis shall be provided in suitable format for use in failure analysis. The critical path shall be designated on topological/layout data which shall be provided in CIF format as well as on circuit and block diagrams. Suitable information on input/output vectors required to properly exercise the critical path signals shall be specified. Additionally, signals expected at each point in the critical path shall be specified and correlated to the respective input/output vector timing sequence. The parameters of these path signals to the input/output vectors and internal nodes shall include the following:

1) Rise and fall times
2) Delay times
3) Frequency/pattern
4) Timing/phase