DATA ITEM DESCRIPTION

Title: Computer Aided Cell Development Data

Number: DI-MCCR-80500A
AMSC Number: 7646
DTIC Applicable: No
Office of Primary Responsibility: NS/I5221
Applicable Forms: N/A

Approval Date: 21 NOV 2006
Limitation: N/A
GIDEP Applicable: No

Use/relationship:

Computer Aided Cell Development Data documents the process for fabrication of integrated circuit cells using computer aids.

Computer Aided Cell Development Data is used by the Government to independently evaluate the reliability of electronic devices fabricated by the contractor.

This Data Item Description (DID) contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated in the contract.

This DID supercedes DI-MCCR-80500.

This DID is related to DI-MCCR-80499A, Computer Aided Chip Development Data.

Requirements:

1.Reference documents.

The applicable issue of the documents cited herein, including their approval dates and dates of any applicable amendments, notices, and revisions, shall be as cited in the current issue of the DODISS at the time of solicitation; or for non DODISS –listed documents, as stated herein.

2. Format and Content:

2.1 The contractor shall prepare and deliver cell development data in accordance with the following:

a) The contractor shall utilize and submit the computer aided cell development data on digital media in the following order of preference:
   i. CD-ROM
   ii. 8mm Helical Scan Tape
   iii. 4mm Digital Audio Tape

The contractor shall utilize electronic media, in accordance with the instructions for digital submissions, for all other documentation and reports.

2.2 Computer Aided Cell Development Data shall be provided in the following formats:

a) Circuit schematic data (identified in Paragraph 3.10d) shall be provided in either SPICE or CDL netlist format. Other formats will be considered with approval at the discretion of the Government Program Manager.

b) Logic equation and/or truth table data (identified in paragraph 3.10f) shall be provided as a simulation model preferably in Verilog or VHDL format. Logic equations are acceptable provided any and all math symbols are defined. Truth tables are acceptable provided all inputs, outputs, and bi-directionals are identified. Truth table columns shall be tab delimited. The contractor shall verify that all input and bi-directional input combinations are accounted for, and that any symbols used in the truth table are defined.

c) Composite layout data (identified in paragraph 3.1.i) shall be provided in the GDSII file (described in DI-IPSC-80409A).

3. Content**:**

3.1. Cell notebook. Consist of data sheets describing each cell. Each sheet contains the following information:

a. Identification. Name and alphanumeric text including date and run number of originating design.

b. Circuit schematic.

c. Logic equation or truth table.

d. Composite layout.

4. END OF DI-MCCR-80500A