DATA ITEM DESCRIPTION

Form Approved
OMB No. 0704-0188

2 TITLE	1. IDENTIFICATION NUMBER
COMPUTER AIDED CELL DEVELOPMENT DATA	DI-MCCR- 80500

3 DESCRIPTION / PURPOSE

3.1 Computer Aided Cell Development Data documents the process for fabrication of integrated circuit cells using computer aids.

3.2 Computer Aided Cell Development Data is used by the Government to independently evaluate the reliability of electronic devices fabricated by the contractor.

4 APPROVAL DATE (YYMMDD)	5. OFFICE OF PRIMARY RESPONSIBILITY (OPR)	6a. DTIC APPLICABLE	6b. GIDEP APPLICABLE
871209	G/S		

7 APPLICATION / INTERRELATIONSHIP

7.1 This data item description (DID) contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated in the contract.

7.2 This DID is related to DI-MCCR-80499 Computer Aided Chip Development Data.

7.3 This DID supersedes DI-E-5369.

8 APPROVAL LIMITATION	9a. APPLICABLE FORMS	9b. AMSC NUMBER
		G4280

10 PREPARATION INSTRUCTIONS

10.1 Content.

10.1.1 Design rules (electrical). Describes the electrical characteristics of the integrated circuit fabrication process. For the metal oxide silicon (MOS) process, this would include threshold voltage, K prime, breakdown voltages, field thresholds, capacitances, and sheet resistivity.

10.1.2 Layout rules. Includes topological rules governing minimum width and spacing of polygons on each level of artwork, permissible via (feedthrough) holes, contacts, and device configurations.

10.1.3 Cell specification (electrical). Includes specifications for circuit performance, including supply voltages, signal levels, propagation time, fan-out, clock rate, clock levels, temperature range, and power dissipation for both nominal and acceptable tolerances.

10.1.4 Cell specification (topological). Includes specifications for overall cell geometries affecting chip layout which contains cell height and width (if constant), permissible device configurations, bus configuration, permissible cell terminal locations, cell interconnection rules, permissible cell overlaps, and cell-to-cell or cell-to-interconnect spacings. (Continued on Page 2)

11. DISTRIBUTION STATEMENT

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited..

Block 10, Preparation Instructions (Continued)

10.1.5 Device library. Includes basic building blocks for custom cell layout, including transistors, resistors, capacitors, contacts and via (feedthrough) shapes. Each component is named and shown in the zero or normal orientation, accurately plotted on a grid whose smallest division represents the smallest resolution required by this process. Indicates variable dimensions with minimum and maximum values of these variables stated.

10.1.6 Cell description data. Shall uniquely describe each cell including the following information:

10.1.6.1 Identification. Cell name and alphanumeric identification.

10.1.6.2 Net list. Connectivity data between devices, terminals, and busses.

10.1.6.3 Placement. Physical locations of devices, terminals, busses, and interconnect.

10.1.6.4 Circuit parameters. Electrical parameters for each device, load capacitances for each net, and coupling capacitances between nets.

10.1.7 Cell parameters. Describes terminal characteristics of each cell. It shall include:

10.1.7.1 Identification. Cell name and alphanumeric identification, including date and run number of originating design.

10.1.7.2 Size. Cell size and reference point.

10.1.7.3 Terminal, bus. Identification, location, interconnect level, capacitance, and linkage to logic simulation.

10.1.7.4 Spacing. To interconnect and other cells from each boundary.

10.1.8 Cell geometries. Describes coordinates of all polygons comprising the cell. Includes identification of cell name, alphanumeric label, date and run number of originating design.

10.1.9 Transient circuit analysis data. Computer listing in contractor format. Listing includes all input data, clearly identified, and relating back to electrical design rules (See 10.1.1), cell specifications (See 10.1.3) and cell description data (See 10.1.6).

10.1.10 Cell notebook. Consists of data sheets describing each cell. Each sheet contains the following information:

a. Identification. Name and alphanumeric text including date and run number of originating design.

b. Clock phase.

c. Drive capability.

Block 10, Preparation Instructions (Continued)

d. Circuit schematic.

e. Logic symbol.

f. Logic equation or truth table.

g. Input formats for chip design programs.

h. Input/output terminal capacitances.

i. Composite layout.

10.2 Format instructions. The Computer Aided Cell Development Data shall be provided in contractor format.