DATA ITEM DESCRIPTION

Form Approved
OMB No. 0704-0188

2. TITLE	1. IDENTIFICATION NUMBER
COMPUTER AIDED CHIP DEVELOPMENT DATA	DI-MCCR- 80499

3. DESCRIPTION/PURPOSE

3.1 Computer Aided Chip Development Data documents fabrication of a chip using computer aids.

3.2 This data product is used by the Government to evaluate the reliability of the integrated circuit device produced by the contractor.

4. APPROVAL DATE (YYMMDD)	5. OFFICE OF PRIMARY RESPONSIBILITY (OPR)	6a. DTIC APPLICABLE	6b. GIDEP APPLICABLE
871209	G/S		

7. APPLICATION/INTERRELATIONSHIP

7.1 This data item description (DID) contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated in the contract.

7.2 This DID is related to DI-MCCR- 80500, Computer Aided Cell Development Data.

7.3 This DID supersedes DI-E-5309.

8. APPROVAL LIMITATION	9a. APPLICABLE FORMS	9b. AMSC NUMBER
		G4279

10. PREPARATION INSTRUCTIONS

10.1 Content and format.

10.1.1 Design rules (electrical). Describes the electrical characteristics of the integrated circuit fabrication process. For the metal oxide silicon (MOS) process, includes threshold voltage, K prime, breakdown voltages, field thresholds, capacitances, and sheet resistivity.

10.1.2 Layout rules. Includes topological rules governing wiring spacing and width, bus configurations and sizes, bonding pad locations, protective devices, spacing-to-borders, test device, identification and alignment marks.

10.1.3 Chip specifications (electrical). Describes chip performance including supply voltages, clock rate and levels, Input/Output (I/O) levels, protective diode characteristics, drive capability, temperature range, and power dissipation for both nominal and acceptable tolerances.

10.1.4 Cell parameters. Describes terminal characteristics of each cell. It shall include:

10.1.4.1 Identification. Cell name and alphanumeric identification, including date and run number of originating design.

10.1.4.2 Size. Cell size and reference point.

(Continued on Page 2)

11. DISTRIBUTION STATEMENT

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

ock 10, Preparation Instructions (Continued)

.1.4.3 Terminal, bus. Identification, location, interconnect level, capacitance, and nkage to logic simulation.

.1.4.4 Spacing. To interconnect and other cells from each boundary.

.1.5 Chip logic diagram. Clearly depicts each I/O terminal, the interconnection path tween cells, and the phase notations. Cross-reference each cell pattern to cell tebook or cell library.

.1.6 Logic simulation printout. Printed output of a logic simulation program ntaining 1s, 0s, and Xs representing the output values of the cells as time is cremented. Printout includes all input data, clearly identified, and run entification, including chip name and descriptive textual data. This listing curately relates back to the logic diagram (see 10.1.5).

.1.7 Testing data.

.1.7.1 Electrical test procedures. Describes all electrical tests to be performed cluding test device measurements, I/O parametric tests, and functional tests.

.1.7.2 Fault detection verification. Consists of a computer listing indicating test quence stimulus/response, type of faults to be detected, test step at which detection s made, and faults which were undetected. Includes all input data, clearly identified r each test run. Accurately relates back to or includes the logic simulation printouts e 10.1.6).

1.8 Chip description data. This data shall uniquely describe each chip. It shall clude:

1.8.1 Identification. Chip name and alphanumeric text.

1.8.2 Logic description. Inputs and outputs for each cell.

1.8.3 Net list. Cell connectivity data which may be derived from logic description.

1.8.4 Placement. Physical location of cells, interconnects, pads, and busses.

1.8.5 Loading. Loading data resulting from fan-out and wiring capacitance.

1.9 Timing analysis printout. Predicted chip performance based on worst-case circuit ding.

1.10 Chip specification (mechanical). Include bonding pad identification, bonding gram, package specifications, labeling instructions, and packing specifications.

1.11 Topological drawing. Printed page plot shall indicate cell, pad, bus, and erconnect locations, ink plots showing cell interconnections, check plots showing line of all geometries, and color overlays of final artwork at 100X. All drawings ll include chip identification, date and job number of originating computer run.

Block 10, Preparation Instructions (Continued)

10.1.12 Cell geometry data. Describes coordinates of all polygons comprising the cell. Includes identification of cell name, alphanumeric label, date and run number of originating design.

10.1.13 Chip geometry data. Describes physical location and orientation of all cells, pads, interconnects, busses, text, and other geometries. When coupled with cell geometry data (see 10.1.12), will completely specify all chip geometries, independent of plotting device.

10.1.14 Artwork generating tape. Tape shall be accompanied by sufficient explanatory text and diagrams to provide data formats, machine type and model, plotting apertures to be used, where applicable, estimated plot time and special instructions to the equipment operator.

10.1.15 Chip artwork. Artwork shall be prepared and provided on dimensionally stable Kodalith Ortho Film 4556, type 3 (.007 inch polyester support), or equal. Artwork shall be 100X positives of the final artwork masters produced under the contract. The 100X identical negatives shall be included. Artwork in the form of 10X reticles may be provided if accompanied by enlargements of the 10X reticles to result in 100X film for each level. Quality of the 10X reticles shall be such that production working plates can be made from them. The artwork shall:

a. Show cells from the cell library, connected and formed into a single chip.

b. Reflect one level of film for each masking step.

c. Contain the identification of each individual level of the chip, including chip name, textual data, date and job number of originating computer run. This data shall physically appear in the border of the 100X artwork.