DATA ITEM DESCRIPTION

Form Approved
OMB No. 0704-0188

1. TITLE	2. IDENTIFICATION NUMBER
Integrated Circuit Chip and Cell Logic Simulation and Test Pattern Verification Report	DI-EDRS-81340

3. DESCRIPTION/PURPOSE

3.1 This data is the documentation of the logical description of each cell and chip used for simulation and test pattern verification of an integrated circuit. This description will include both the normal and faulted configurations of each cell and chip.

4. APPROVAL DATE (YYMMDD)	5. OFFICE OF PRIMARY RESPONSIBILITY (OPR)	6a. DTIC APPLICABLE	6b. GIDEP APPLICABLE
930701	G/Y27		

7. APPLICATION/INTERRELATIONSHIP

7.1 This Data Item Description (DID) contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated in the contract.

7.2 This data item interrelates with DI-MCCR-80499 and DI-MCCR-80500.

8. APPROVAL LIMITATION	9a. APPLICABLE FORMS	9b. AMSC NUMBER
		G6930

10. PREPARATION INSTRUCTIONS

10.1 Format. The report shall be prepared using on 8 1/2 x 11 inch paper. Throughout this data item the term the term "cell" shall be defined as "a primitive logic element"; e.g., Inverter, NAND, NOR, flip-flop, etc., and shall not include complex functions such as counters, registers, etc.

10.2 Contents. The Integrated Circuit Chip and Cell Logic Simulation and Test Pattern Verification report shall include:

a. A description of the type of faults to be detected.

b. A brief description of the computer program and or manual technique used in the simulation and test pattern verification shall be provided and shall include:

(1) The name of the computer program and, if available to the Government, where it can be obtained.
(2) The data and revision of the program used.
(3) The number of faulted and normal states that can be simulated or verified, e.g. 0, 1, X, etc.

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11. DISTRIBUTION STATEMENT

DISTRIBUTION STATEMENT A: Approved for public release; distribution is unlimited.

Block 10, Preparation Instructions (Continued)

(4) A description of the conditions required for a fault to be considered detected.

(5) A complete list of assumptions made (if applicable) in modeling cells and performing chip simulations and test pattern verifications.

(6) A complete description of the logic implementations of each cell shall be provided. This description shall include:

a. Logic diagram describing logical implementation.
b. Logic truth table including the normal and faulted conditions.
c. A list for each cell of any normal or faulted condition not included in the logical model due to limitations in the computer program manual technique, etc.

c. The listing(s) of the chip simulation and test pattern verification shall be provided. Sufficient data shall be provided with the listing to enable the Government to interpret the form and format of the listing(s). This listing(s) shall include:

(1) The input stimulus and response of the normal or unfaulted condition of the chip. This stimulus shall be identified to the input used in test pattern verification.

(2) A list of the undetected faults clearly identified and traceable back to the chip
logic diagram.

(3) The percent test pattern grading level achieved with the input stimulus provided.