DATA ITEM DESCRIPTION

Title: VHSIC Hardware Description Language (VHDL) Documentation

Number: DI-EGDS-81729
AMSC Number: 7684
DTIC Applicable: No
Office of Primary Responsibility: NS/I1S4
Applicable Forms: N/A

Approval Date: 20 DEC 2006
Limitation: N/A
GIDEP Applicable: No

Use/Relationship:

VHDL documentation contains behaviors and structural descriptions of an electronic system, subsystem, or device. The primary purpose of these data items is to document hardware designs in a machine processable, simulatable, and hierarchical format.

This Data Item Description contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated in the contract.

The contract will provide a list of Government approved leaf level modules and a list of VHDL language definitions. The Contracting Officer Technical Representative is responsible for monitoring the status of the list of Government leaf level modules and preparing contract modifications to reflect current leaf level module requirements in the contract.

The DD Form 1423 (Block 16) will contain the requirements for preparation of the deliverable VHDL documentation. The preferred means of delivering all VHDL documentation shall be machine-readable ASCII files contained on specific magnetic media and in the machine format required by the Government Activity user. ASCII files are defined as those satisfying character set requirements of the VHDL Language Reference Manual. Requirements for preparation of deliverable hard copy (printed-paper media) documentation shall also be provided on the DD Form 1423 (Block 16). The preferred documentation shall be comprised of:

a. Nine-track magnetic tape, 1600 bits per inch, unlabeled, 80-character records, and a blocking factor 1920 (i.e., 24, 80-character records per block). A label containing text identifying the tape contents shall be affixed to the tape reel.

b. Hard copy (printed on paper) containing the machine loading instructions and the contents of the file #1 and file #2 on the tape (Section XXX).

Requirements:

1. Reference Documents. The applicable issue of the documents cited herein, including their approval dates and dates of any applicable amendments, notices, and revisions, shall be as stated herein.

   1.1 VHDL Manual.
   IEEE Standard VHDL Language Reference Manual, IEEE Std. 1076-1987.
   The Institute of Electrical and Electronics Engineers, Inc.
   345 East 47th Street, New York, NY 10017, USA

2. VHDL Documentation Format. Each file delivered under contract shall be either VHDL design file, whose entire contents conform to the requirements of the VHDL Language Reference Manual (including the definition of comments), or an auxiliary information file, containing no VHDL design units. Design units which are new with the contractual deliverable shall not be contained in the same design file with the design units which have been previously accepted by the Government. The sequential order of the files of the deliverables shall be:

   a. File #1: Names of all files of the deliverable VHDL documentation, named in accordance with the originating host operating system; one file name per record and nothing else (pad with trailing blanks).

   b. File #2: High-level prose overview of the VHDL description that cites contract, line item, Contract Data Requirements List sequence number, and summarizes the organization and content of the set of files.

   c. File #3: Specification of a sequence for analyzing the VHDL design units of the deliverable that is consistent with the order of analysis rules in the VHDL Language Reference Manual.

   d. File #4: List of VHDL modules which were selected from the Government list of leaf level modules.

   e. File #5: List of VHDL modules which are revisions of modules previously accepted by the Government.

   f. File #6: List of VHDL modules which originate with the VHDL delivery.

   g. File #7: List which associates VHDL modules with their corresponding test benches.

   h. File #8 et seqq.: Auxiliary information files concerning the VHDL descriptions and VHDL design files. Auxiliary information files shall precede VHDL design files.

3. VHDL Documentation Content. VHDL documentation contains behavioral and structural descriptions of the hardware being documented and behavioral descriptions of the VHDL test benches required to demonstrate their functionality.

3.1 VHDL Module Hierarchy. A VHDL description for the hardware shall be a hierarchy of VHDL modules, analogous to the physical hierarchy of the hardware being documented. A VHDL module consists of a VHDL entity declaration, one or more behavioral VHDL bodies, and except for allowable leaf level modules, a structural VHDL body. One VHDL module shall be defined for the entire system and one for each physical electronic unit (assembly, subassembly, integrated circuit, etc.) of the hardware system. VHDL modules should also be defined for important subsections or groupings of complex physical units (e.g., macrocells of a chip or boards defining a processor).

3.1.1 Allowable Leaf Level Modules. Leaf level modules are VHDL modules for which no VHDL structural body is required. The only permitted leaf level modules are:

a. Modules selected from a Government list of leaf level modules referenced or contained in the contract.

b. Modules corresponding to a collection of hardware elements which together exhibit a stimulus response behavior, but whose interaction is best modeled at the electrical or physical level. Examples of such modules are digital logic gates, analog circuit blocks, and power supplies.

c. Modules whose detailed design has not yet been completed but whose behavior is required as a delivery disclosure at specified times during the contract.

3.2 Entity Declaration. The entity declaration for each module shall include an interface declaration, timing and electrical requirements for the behavior of the device, allowable operating conditions, component identification, and explanatory comments.

3.2.1 Interface Declaration. The interface declaration for each entity shall describe all input and output ports. The interface description shall include information which relates each input and output port to a package pin number or connector pin number whenever such a correspondence exists. This information may be in the form of port attributes or port mapping statements which relate functional port names with connector pin numbers.

3.2.2 Timing and Electrical Requirements. Timing and electrical requirements (e.g., setup and hold times or power supply voltage extremes) shall be expressed in such a manner as to cause the simulator to generate error messages should the requirements be violated during a simulation.

3.2.3 Operation conditions. Operating conditions are the physical and electronic environment in which physical components are designed to operate, such as temperature range, signal excursions, logic level definition, maximum power dissipation, radiation hardness, etc. VHDL package declarations should be used whenever operating conditions are common across a class of similar components.

3.2.4 Entity Naming Conventions. Names for VHDL entities shall be traceable to the names of physical electronic counterparts whenever such a correlations exists.

3.3 Behavioral Body. A behavioral body is an abstract, high-level, VHDL description which expresses the function and timing characteristics of the corresponding physical unit. All user programmable registers should be clearly identifiable in the simulation model. Test and maintenance functions which are part of the physical units and are available to the user shall be included in the behavioral body. Data flow, procedural and structural constructs may be used for expressing behavior.

3.3.1 Decomposition of Behavioral Bodies. Structural decomposition of behavioral bodies shall be used only to show functional partitions which are not clear from the partitions of the corresponding structural body. When determining the appropriate level of hierarchical decomposition, ease of simulation and clarity of behavior should be kept in mind. For example, it may be appropriate to decompose a computer which is made up of several bit-slice micro-processors into composite arithmetic logic units and register files which span portions of several chips. However, decomposing it into Boolean logic primitives (e.g., AND and OR operators) would neither clarify the behavior of the system nor make it easy to simulate.

3.3.2 Timing Characteristics. Signal delays at output ports of the VHDL modules shall accurately model the behavior of the physical units corresponding to the VHDL modules. Best, worst, ad nominal output delays shall all be included. More elaborate timing models which take into account other variables such as supply voltage or output loading may also be used.

3.3.3 Structurally Dependent Signal Values. Signal values which are dependent on a particular structural implementation, such as scan path signatures, shall not be specified in the behavioral module.

3.4 Structural Body. A structural VHDL body is composed exclusively of interconnected lower level components. Structural bodies shall represent the physical implementation accurately enough to permit logic fault modeling and test vector generation. Structure which is created to support testing and maintenance such as scan paths shall be included in the VHDL structural description.

3.4.1 Structural Naming Conventions. For ease of schematic drawing correlation, and within the constraints of the lexical rules of VHDL, names for components and signals shall be the same as, or traceable to, their electrical schematic counterparts.

3.5 VHDL Simulation Support. VHDL test benches which simulate the correct behavior of each VHDL module required by the contract to be simulatable as stand alone module shall be furnished and clearly distinguished from the VHDL modules representing the design itself.

3.5.1 VHDL Test Benches. A VHDL test bench is a collection of VHDL modules which apply to stimuli to a module under test (MUT), compare the MUT's response with an expected output, and report any differences between observed and expected responses during simulation. VHDL configuration information required to simulated the MUT shall be included with the test bench.

3.5.2 Test Requirement Correlation. VHDL test benches shall be cross-referenced to the contractually required hardware test plans, specifications and drawings.

3.5.3 VHDL Test Bench Completeness. Every VHDL module of the hardware hierarchy shall be simulatable as a stand alone module and hence a corresponding VHDL test bench is required for every VHDL module of the hierarchy.

3.6 Error Messages. Error messages generated anywhere in either the VHDL description of the actual hardware or the test bench should identify the requirement which has been violated and the name of the VHDL design unit in which the error occurred. Applicable VHDL design units include: entity declarations, structural and behavioral bodies, package declarations, package bodies, and configurations.

3.7 Annotations. VHDL design units shall include explanatory comments which augment the format VHDL text to make the intent of the VHDL model clear. The following information is required:

a. Any factors restricting the general use of this description to represent the subject hardware.

b. General approaches taken to modeling and particularly decisions regarding modeling fidelity.

c. Any further information which the originating activity considers vital to subsequent users of the descriptions.

3.8 Reference to Origin. Included in the VHDL documentation shall be a list of VHDL modules new with this deliverable and a list of VHDL modules that have been used without change modules selected from the list of Government VHDL modules referenced in the contract. Those modules included from previously existing descriptions shall include:

a. Identification of originator or source
b. DOD approved identifier (if one exists)
c. Design unit name/revision identifier

3.8.1 Revision Management. VHDL design units, once accepted by the Government, shall be revised only with approval of the Contractor Officer. A design unit revision history shall be included in comments in each revised design unit. The revision history shall include: the date of revision, the performing individual and organization, the rationale for the revision, a description of where the original design unit required modification and the testing done to validate the revised model.

4. END OF DI-EGDS-81729