DATA ITEM DESCRIPTION

Form Approved
OMB No. 0704-0188

1. TITLE	2. IDENTIFICATION NUMBER
Integrated Circuit Cell/Functional Sub-Block Data Notebook	DI-EDRS-81339

3. DESCRIPTION/PURPOSE

3.1 This data is to be prepared in the process of developing an integrated circuit cell/functional sub-block standard library.

3.2 This data will be used to document these cells/functional sub-blocks in detail sufficient to perform artwork topological design rule checking, circuit analysis, cross

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4. APPROVAL DATE (YYMMDD)	5. OFFICE OF PRIMARY RESPONSIBILITY (OPR)	6a. DTIC APPLICABLE	6b. GIDEP APPLICABLE
930701	G/Y27		

7. APPLICATION/INTERRELATIONSHIP

7.1 This data item description contains the format and content preparation instructions for the data product generated by the specific and discrete task requirement as delineated by the contract.

7.2 Used on programs where either cost/schedule control system criteria, in accordance with DOD Instruction 7000.2, or cost/schedule planning and control system requirements are to be applied.

8. APPROVAL LIMITATION	9a. APPLICABLE FORMS	9b. AMSC NUMBER
		G6929

10. PREPARATION INSTRUCTIONS

10.1 Reference documents. The applicable issue of the documents cited herein, including their approval dates and dates of any applicable amendments, notices and revisions, shall be as specified in the contract.

10.2 Format. The document shall be prepared on 8 1/2 x 11 inch paper using nonfading ink suitable for reproduction. This document shall be bound together between a rigid binder.

10.3 Content. The Notebook shall contain the following data for each cell/functional sub-block used on or developed for use in the design of integrated circuits whether prepared by automated layout, digitizing, interactive graphics, or manual layout.

a. Title Page
b. Index
c. Design Criteria/ Objectives and Analysis Description
d. Design Rules: (1) Electrical (2) Topological
e. Cell/ Functional Sub-Block Data Sheet

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11. DISTRIBUTION STATEMENT

DISTRIBUTION STATEMENT A: Approved for public release; distribution is unlimited.

Block 3. Description/Purpose (Continued)

referencing to the logic symbol and logic diagram, and as an engineering document to be used in the design of integrated circuits using these cells/functional sub blocks

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Block 10, Preparation Instructions (Continued)

10.4 Title Page. The Title Page shall contain the following information:

a. Contract Short Title
b. Contract Number
c. Contractor Name and Address
d. Integrated Circuit Technology Name
e. Date Prepared

10.5 Index. An index reference by page number shall be prepared to facilitate location of material contained in the document.

10.6 Design Criteria/Objectives and Analysis Description. This section shall contain a detailed description of the design criteria/objectives, the analysis performed to meet these objectives, and the results of the analysis. The design criteria/objectives shall describe the goals in areas such as frequency, propagation delay, drive capabilities, noise immunity, supply voltages ranges, input and output levels, unique interface constraints, clock levels and waveforms, cell/functional sub-block fanout or levels of propagation constraints, etc. The analysis performed during design shall be described along with the results of the analysis demonstrating the design goals have been met. Where computer modeling of circuits are used in the analysis, a description of the model and modeling equations along with the process parameters used in the analysis shall be described.

10.7 Design Rules. This section shall describe the semiconductor process electrical parameters limits (min, max, typical values) over which the cells/functional sub-blocks are designed to operate. It shall also contain a description of the topological design rules used in the layout of the cells/functional sub-blocks.

10.8 Data Sheets. The data sheet shall contain the following information:

a. Cell/functional Sub-Block Number. The cell/functional sub-block's number shall be consistent with the numbering used on other integrated circuit data items (i.e., logic diagram and composite/map).

b. Schematic Circuit Diagram. This shall show the interconnection of transistors, resistors, etc., which make up the cell /functional sub-block. The transistor device sizes, resistor values, etc., shall be labeled. The input/output connections shall be labeled and shall correspond with the labeling on the logic symbol and logic diagrams for cross-referencing one to the other.

Block 10. Preparation Instructions (Continued)

c. Cell/Functional Sub-Block Logic Symbol. Using ANSI-Y32.19, Graphic Symbols for Logic Diagrams, shall be the symbol used on the logic diagrams used to specify the logical function of the integrated circuit. The input/output connections shall be labeled and shall correspond to labeling used on the logic diagram. This is to be used for cross referencing and determining the actual as built interconnections of the cells/functional sub-blocks on the chip on a one for one basis. The above applies to digital integrated circuits.

d. Logic Equation or Truth Table. The logic equation or truth table for the cell/ functional sub-block shall be shown.

e. Input Output Terminal. Capacitances or performance Curve. The input and output capacitances of the cells/functional sub-blocks shall be specified. If appropriate, performance or propagation delay curves shall be shown.

f. Design or Usage Notes. Any restrictions or usage notes or comments shall be specified on the data sheet. Items such as clock phase for phased logic cells, special power connections, etc., shall also be specified.